Honeywell

SERIES 16

DDP-516 GENERAL PURPOSE COMPUTER THEORY OF OPERATION AND MAINTENANCE VOLUME I

Doc. No. 70130071620J Order No. FT76

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JANUARY 1972

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DDP-516 GENERAL PURPOSE COMPUTER

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DDP-516 General Purpose Computer

CHAPTER I
INTRODUCTION

SCOPE OF MANUAL

The DDP-516 Instruction Manual consists of three volumes the contents of which are as follows:

1) Volume I, theory of operation and maintenance information for the computer central processor logic, computer memory and standard input/output (I/O) equipment interface.

2) Volume II, instruction analysis with supporting flow charts and timing diagrams and a function index listing.

3) Volume III, computer central processor logic and power distribution diagrams, memory logic diagrams and mechanical coding drawings.

APPLICABLE DOCUMENTS

All manuals provided as standard documentation with each DDP-516 computer are listed in Table 1-1.

The documentation package provided with each DDP-516 system includes all the documents listed in Table 1-1. Customers may obtain additional copies of any manual by contacting their local Honeywell Inc. Computer Control Division representative or by writing directly to:

Honeywell Inc.
Computer Control Division
Old Connecticut Path
Framingham, Massachusetts 01701

Table 1-1.
Standard DDP-516 Documentation

Title	Document No.
Hardware Manuals	
Instruction Manual for DDP-516 General Purpose Computer	
Volume I, Theory of Operation and Maintenance	130071620
Volume II, Instruction Analysis and Timing/Flow Diagrams	130071621
Volume III, Drawings	130071622
Installation Manual for DDP-516 General Purpose Computer	130071625
Interface Manual for DDP-516 General Purpose Computer	130071624

Table 1-1. (Cont)
Standard DDP-516 Documentation

Title	Document No.
Hardware Manuals (Cont)	
Automatic Send-Receive Teletypewriter Set (ASR) Teletype Corp. (See note)	
Model 35, Bulletin 280 B Volume 1 and Bulletin 280 B Volume 2	
Model 33, Bulletin 273 B Volume 1 and Bulletin 273 B Volume 2	
Software Manuals	
Programmers Reference Manual for DDP-516 General Purpose Computer	130071585
Programmers Reference Card for DDP-516 Computer	130071623
Input/Output Library for DDP-516 Computer	130071631
Math Library for DDP-516 Computer	130071632
Utility Programs for DDP-516 Computer	130071635
Test Programs for DDP-516 Computer	130071633
Assembly Program Manual for DDP-516 Computer	130071629
FORTRAN Systems Manual for DDP-516 Computer	130071634
Users Guide for DDP-516 Computer	130071627

NOTE

Both the Model 33 and 35 ASR units are available as standard I/O devices; the model unit used for a system is determined by the customer.

GENERAL DESCRIPTION

The DDP-516 computer is a solid-state, 16-bit binary word, general purpose computer with an internally stored program, a 0.96 μsec memory cycle time and a memory expandable from 4K to 32K. The machine has a fully parallel organization, and both indexing and multi-level indirect addressing capabilities. Standard features include a flexible repertoire of 72 commands, a powerful I/O bus structure, standard teletype I/O equipment and a full line of options and optional peripheral devices.

The 16-bit word allows a straightforward and efficient "sectorized" addressing scheme. The use of large sectors permits most instructions to be coded in one word each. The 16-bit machine word is directly compatible with the ASCII 8-bit character code.

The overall characteristics of the DDP-516 computer are given in Table 1-2.

Table 1-2.
Leading Particulars

Primary Power	1.4 kw at 115 vac ±10% at 60 cps ±2 cps
Type	Parallel binary, solid state
Addressing	Single address with indexing and indirect addressing
Word Length	16 bits (single precision) 31 bits (double precision)
Machine Code	Two's complement
Circuitry	Integrated
Signal Levels	Active: 0v Passive: +6v
Memory Type	Coincident-current ferrite core
Memory Size	4K, 8K, 12K, or 16K (Optionally expandable to 32K)
Memory Cycle Time	0.96 μsec
Instruction Complement	72 instructions
Speed	
Add	1.92 μsec
Subtract	1.92 μsec
Multiply (optional)	5.28 μsec
Divide (optional)	10.56 μsec (max)
Standard Memory Protect	Designed to protect memory data in the event primary power fails
Standard Interrupt	Single standard interrupt line
Input/Output Modes	Single word transfer Single word transfer with priority interrupt Direct multiplexed control (optional) Direct memory access control (optional)
Standard I/O Lines	10-bit address bus 16-bit input bus 16-bit output bus external control and sense lines
Standard Teletype	Read paper tape at 10 cps Punch paper tape at 10 cps Print at 10 cps Keyboard input Off-line paper tape preparation, reproduction and listing
Dimensions (less console)	24 in. x 24 in. x 38 in.
Weight	250 lb
Environment	Room ambient for computer less I/O devices: 0°C to 45°C
Cooling	Filtered forced air

Computer Operations

The main access paths for data and command words in the DDP-516 computer are shown in simplified form in Figure 1-1. As shown, the computer consists of control logic for the development of clock, control and enable levels; memory for the storage of data, and a series of registers (M, X, P, etc.) which are used for actual handling and processing of data. The computer is also supplied with a separate control console which is used for the manual entry of data into the computer, the control of the operations to be performed and the display of data and operational information.

The gating of data between the registers of the computer is performed by adder gating logic and by the D-Register. Data transfers to and from the computer are performed by an input/output structure consisting of:

1) an address bus (ADB)
2) an output bus (OTB)
3) an input bus (INB)
4) control signals.

A detailed description of the computer, central processing logic, memory systems, and I/O structure for standard devices is presented in Chapter II, Sections 1, 2, and 3, respectively. Detailed information regarding the programming, interfacing and installation of the DDP-516 computer is presented in other manuals of this series (refer to Table 1-1).

PHYSICAL DESCRIPTION

The basic DDP-516 equipment enclosure consists of a small desk-height unit shown in Figure 1-2. This unit is capable of housing one fixed power supply and distribution assembly, and two tilt-out assemblies. The unit is 37 3/4 in. high, 24 in. wide, 25 5/8 in. deep and weighs approximately 250 lb. A front view of the unit with the front access door open is illustrated in Figure 1-3; this view shows the location of the power supply and tilt-out assemblies contained in the basic unit. Figure 1-4 illustrates the manner in which the tilt-out assemblies may be positioned for access to the equipment which they contain.

In a minimum (single-bay) system only one enclosure (bay) is used; two and three bays are used, respectively, for intermediate and maximum DDP-516 system equipment configurations. In multi-bay systems, the enclosures are bolted together to form a single rigid enclosure.

Control Console Unit

A separate control console unit supplied with the system contains all of the manual controls and displays. This unit may be placed on top of the basic equipment enclosure (see Figure 1-2), or any other suitable work surface; its placement is restricted only by the length of the console/computer interconnecting cable. The use of the controls and indicators contained in this unit is described in the Programmers Reference Manual.

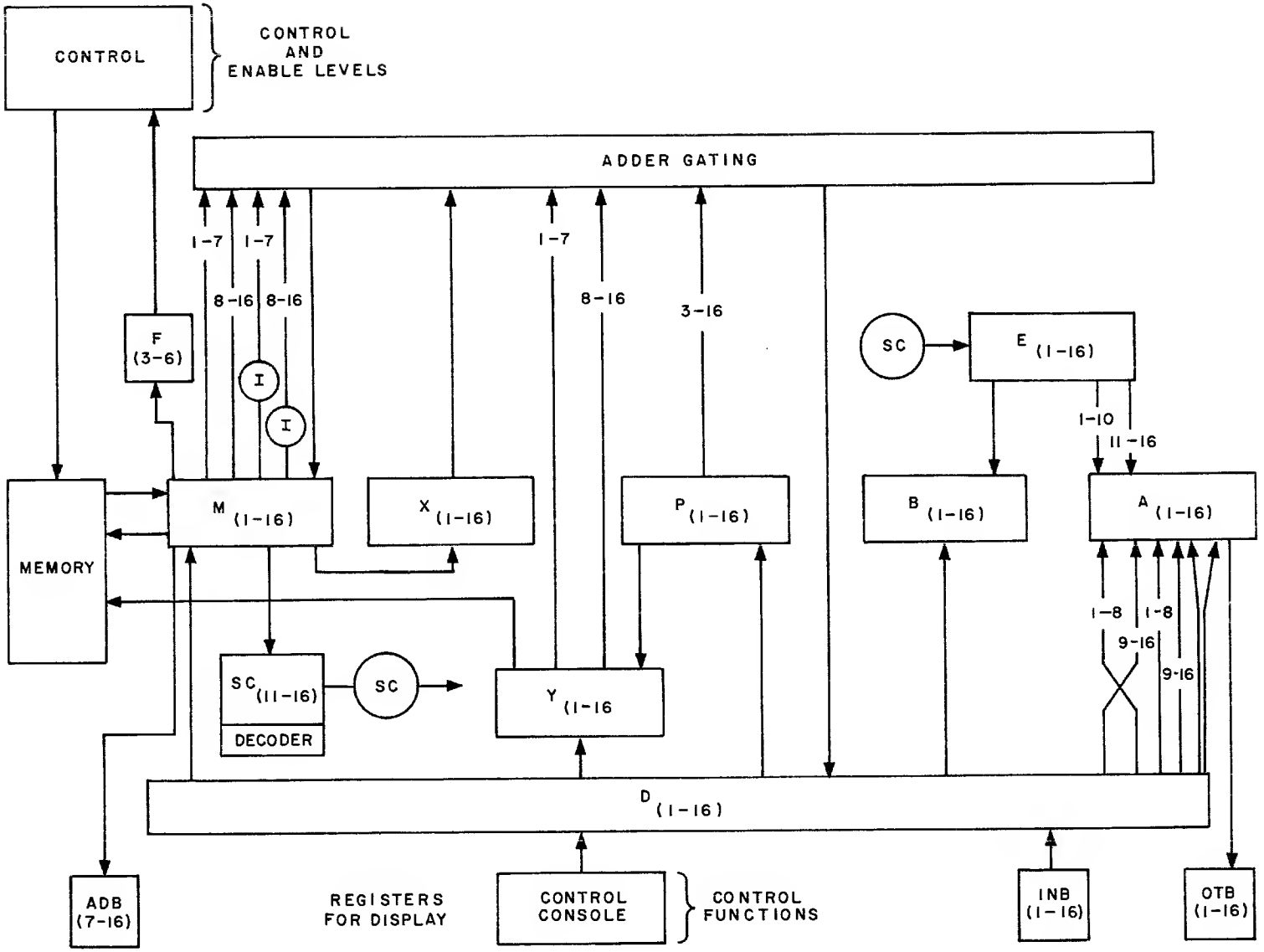


Figure 1-1. DDP-516 General Purpose Computer, Simplified Block Diagram

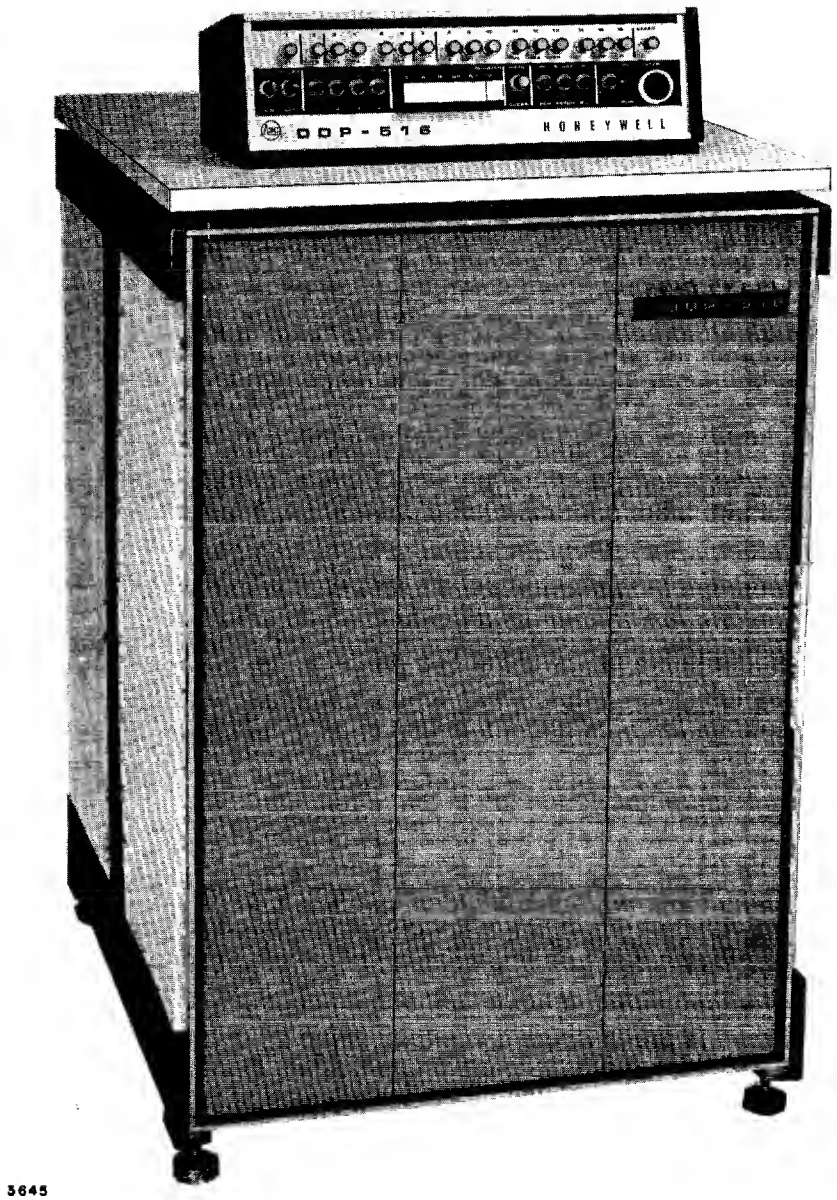


Figure 1-2. Basic (Single-Bay) Equipment Enclosure with Control Console Unit

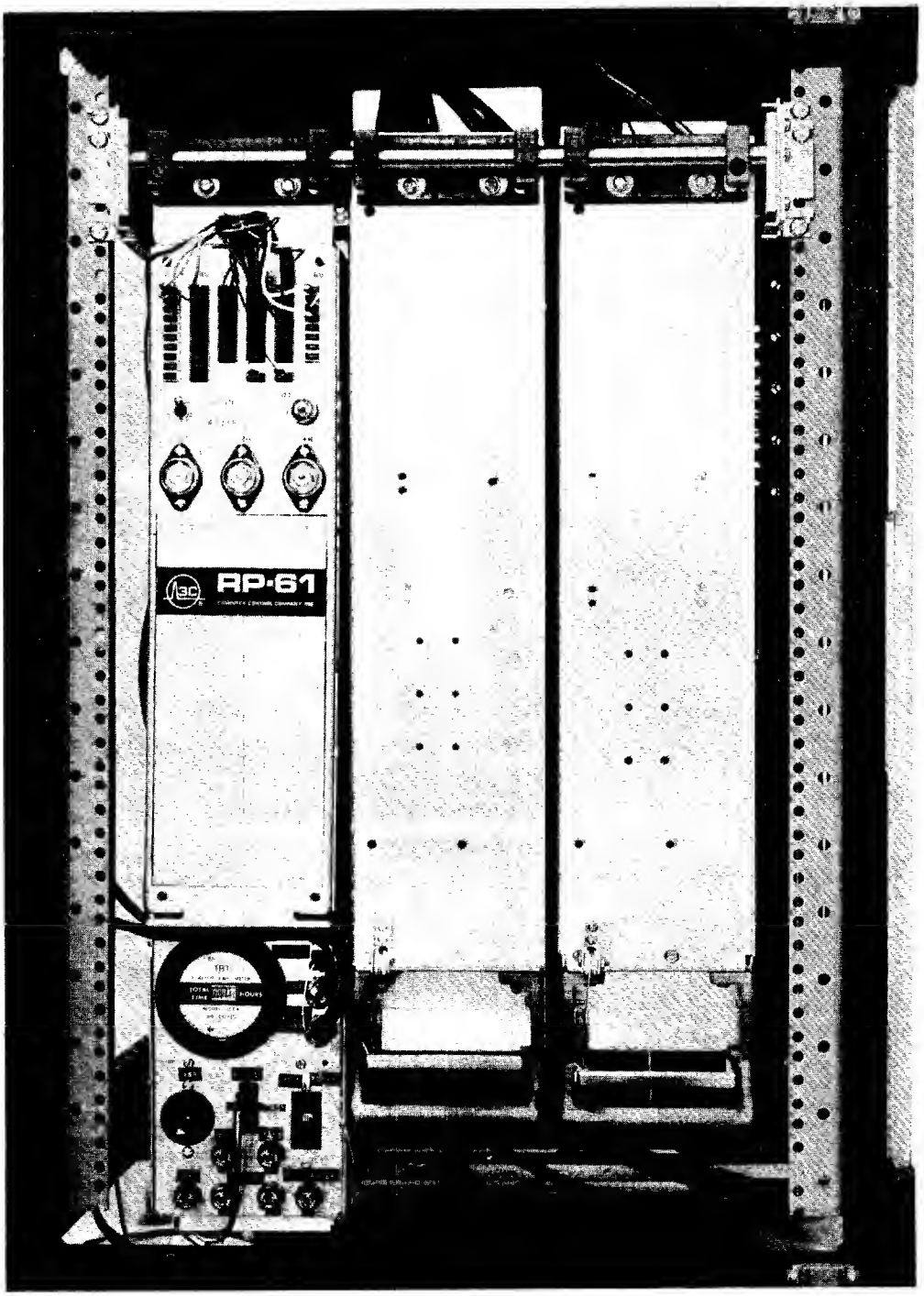


Figure 1-3. Typical Equipment Bay, Front View

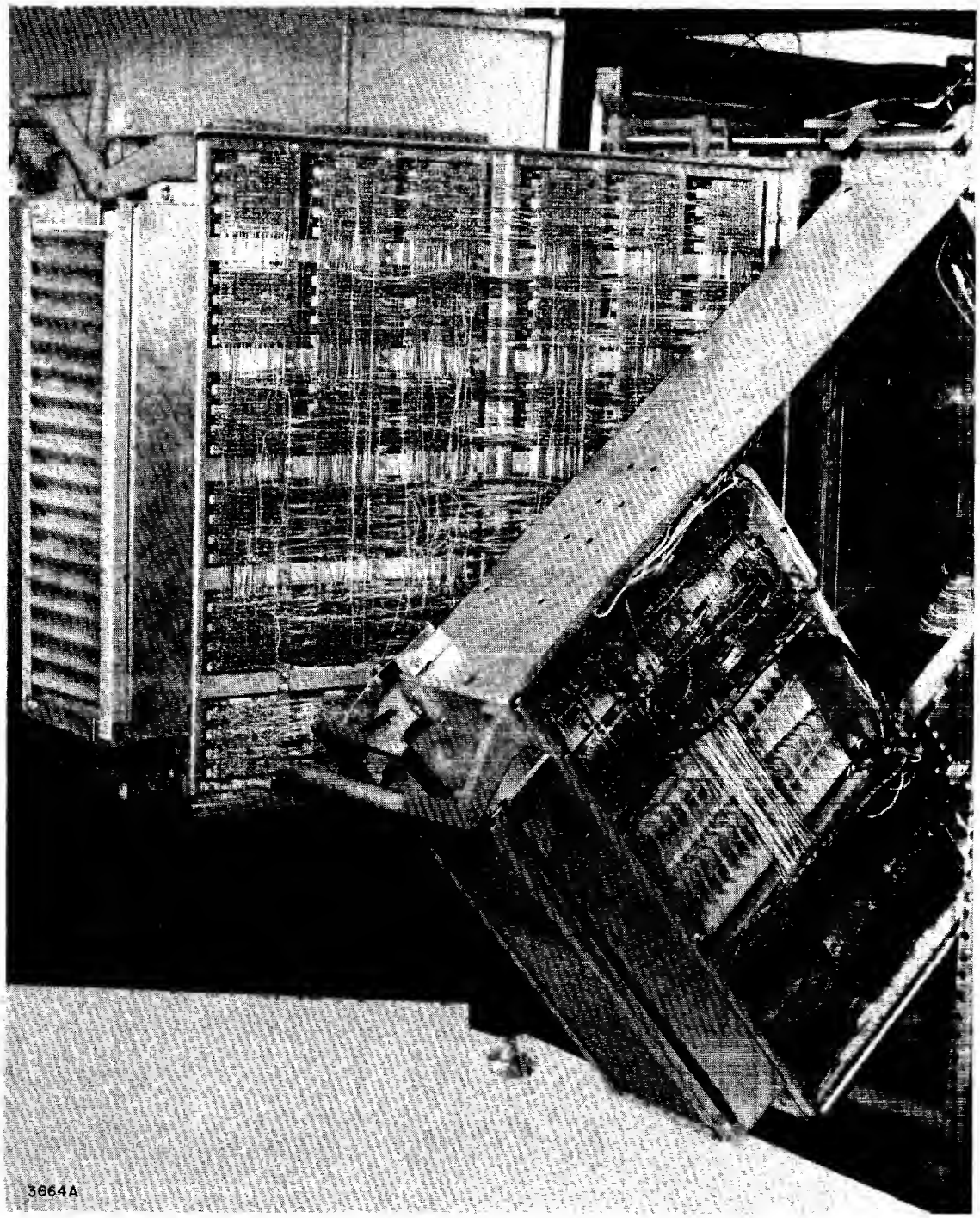


Figure 1-4. Positioning of Tilt-Out Assemblies

PAC COMPLEMENT

Table 1-3 lists the type and quantity of the μ-PAC integrated circuit modules used in the basic DDP-516 computer. These μ-PACs are housed in the tilt-out assemblies provided in the basic system equipment enclosure. The μ-PAC layout for the computer central processing unit (CPU) and the memory are contained in Volume III of this manual.

The μ-PAC modules listed in Table 1-3 are described in the appendix of this volume.

Table 1-3.
Basic Computer, μ-PAC Complement

Type		Quantity
CC-002	Driver Matrix	6
CC-034	Carry Most Significant Bits	1
CC-035	Carry Middle Bits	1
CC-036	Carry Least Significant Bits	1
CC-037	Column BEX	8
CC-038	Column Memory Information Register and Distribution Register	16
CC-039	Column PAY	8
CC-043	Power Failure Sense	1
CC-044	Priority PAC	1
CC-045	NAND Power Amplifier Type I	4
CC-046	Master Clock	1
CC-054	Pin Jumper PAC	5
CC-073	NAND Power Amplifier Type II	6
CC-079	Cable PAC	1
CC-080	Cable PAC	1
CC-085	Universal Flip-Flop	3
CM-003	Timing Distribution	2
CM-006	Selection PAC	34
CM-022	Parallel Transfer Gate	2
CM-032	Sense Amplifier	8*
CM-033	Sense Amplifier	8**
CM-075	Component PAC	1
CM-106	Selection PAC	4***
DC-335	Multi-Input NAND PAC	9
DI-335	NAND Type I PAC	12
DL-335	NAND Type II PAC	20
DN-335	Expandable NAND PAC	6
OD-335	Octal/Decimal Decoder PAC	2
PA-335	Power Amplifier PAC	4
PA-336	Power Amplifier PAC	12
TG-335	Transfer Gate PAC	10

*Used for 4K Memories Only
**Used for 8K Memories Only
***Six are required for an 8K Memory

CHAPTER II
THEORY OF OPERATION

The following information is organized to supplement and complement the flow charts and instruction analyses of Volume II and the logic diagrams of Volume III of this manual. A discussion of the overall operational sequences is based on a master flow chart that is a condensation of the fully detailed flow charts of Volume II. Included in this section are discussions dealing with data and command word formats, basic modes of operation, and the processes involved in instruction fetching, address modification and execution.

SECTION 1 - CENTRAL PROCESSING UNIT (CPU)

A discussion of the central processor (CPU) data flow, based on an overall block diagram, introduces the control signals that appear most frequently on the flow charts of Volume II. Complex logic structures, such as the adder, and clock system, are described in detail.

FORMAT AND EXECUTION OF INSTRUCTIONS

Word Structure

Data Words. -- Data words are stored in binary form using two's complement notation. The DDP-516 accepts and processes data words in both single and double precision. Single-precision data words (Figure 2-1) include 15 magnitude bits plus a sign bit and represents a data range of $\pm 2^{15}$ or $\pm 32,768$.

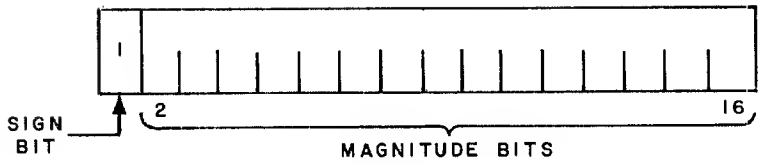


Figure 2-1. Data Word Format, Single-Precision

Double-precision data words (Figure 2-2) include two data words, each one having 15 magnitude bits. The first data word includes the 15 most significant bits (MSB) of the number plus a sign bit. It is identical to a data word using single-precision. The second data word includes the 15 least significant bits (LSB) of the double-precision word. The sign position is always zero. Double-precision data words represent a data range of $\pm 2^{30}$ or ±1,073,741,824.

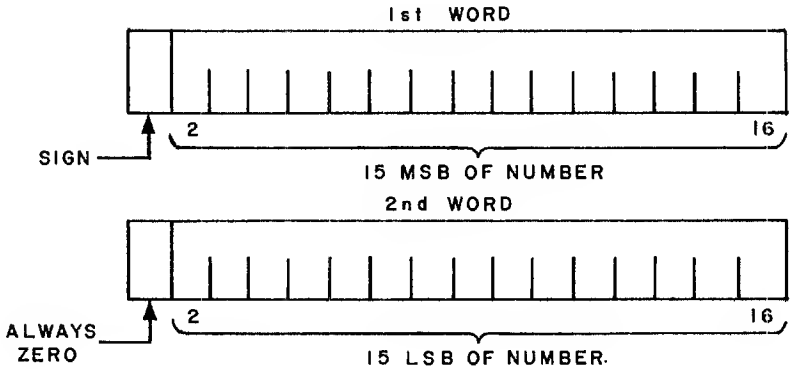


Figure 2-2. Data Word Format, Double-Precision

Instruction Words. -- There are four types of instruction words:

a. Memory reference
b. Generic
c. Input/output
d. Shift

The memory reference instructions are identified by a format as shown in Figure 2-3. Bit 1, the flag bit, denotes indirect addressing; bit 2, the tag bit, denotes indexing; bits 3 through 6 denote the operation code (Op Code); bit 7 is the sector bit; and bits 8 through 16 denote the address.

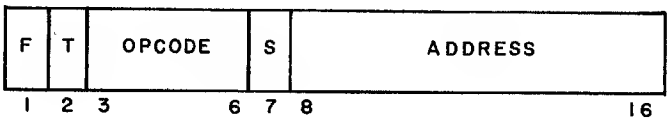


Figure 2-3. Memory Reference Instruction Format

Generic instructions are identified by a word format as shown in Figure 2-4. Bits 1 through 16 denote the Op Code.

Figure 2-4. Generic Instruction Format

Input/output instructions are identified by a word format as shown in Figure 2-5. Bits 1 through 6 denote the Op Code and bits 7 through 10 denote the type of function to be performed. The I/O device is specified by bits 11 through 16.

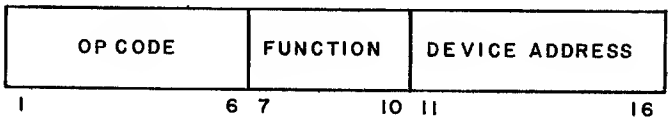


Figure 2-5. Input/Output Instruction Format

The shift instructions are identified by a word format as shown in Figure 2-6. Bits 1 through 10 denote the Op Code and bits 11 through 16 contain the two's complement of the number of shifts to be performed.

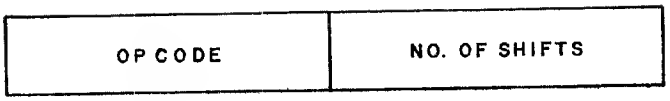


Figure 2-6. Shift Instruction Format

MEMORY ADDRESSING MODES

The following discussion applies to memory sizes up to 16,384 words. For larger memories, reference should be made to the Extended Addressing Option Manual, 3C Doc. No. 130071646.

The memory address is formed in $(Y)_{3-16}$. Bits 1 and 2 of the Y-register are ignored.

Figure 2-7 is an illustration of the memory sectors in a 4096 word memory. Each sector has 512 words. There are fifteen dedicated memory locations reserved for a fill program. They are located at $(00001)_8$ through $(00017)_8$. These locations can only be altered by using the memory access mode from the console. The logic which protects these locations is shown on LBD 126. A power failure causes an interrupt to location $(00060)_8$ and the standard interrupt link is at location $(00063)_8$. The power failure logic is shown on LBD 135.

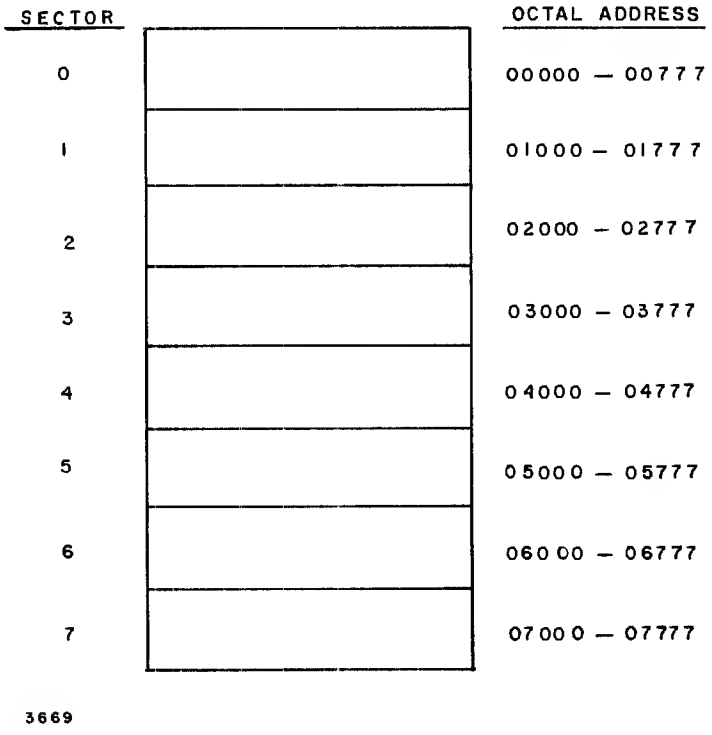


Figure 2-7. Memory Section in a 4096-Word Memory

The standard memory reference instruction word format allows 10 bits for addressing. Nine of these ten bits are used to specify any location within a given sector. The remaining bit (called the sector bit) specifies this particular sector as sector zero or the sector currently being accessed by the P-register.

For a 16,384 word memory, 14 bits of addressing are necessary. The least significant 9 bits of this address are provided by the instruction word. The most significant five bits are either extracted from the P-register (if the sector bit is a ONE), or are zeros (if the sector bit is zero). This mechanism allows any memory reference instruction to directly address any of 1024 words.

There are two mechanisms for addressing a sector other than sector zero or the P-register sector. They are indexing and indirect addressing. Indexing adds the contents of the X-register (14 bits) to the address specified by the instruction word. Indexing is specified by bit 2 of the instruction word.

Indirect addressing uses the address specified by the instruction word to fetch a new 14-bit address. Indirect addressing is specified by bit 1 of the instruction word.

Direct Addressing

Sector Bit Zero (See Figure 2-8). -- When sector bit M07 is ZERO, a 9-bit address specified in bits 8 through 16 of the M-register (instruction word) specifies any location in sector 0. $(Y)_{8-16}$ are loaded from $(M)_{8-16}$ and $(Y)_{1-7}$ are cleared.

Sector Bit One. -- With the sector bit a one, a 14-bit address specified in bits 8 through 16 of the M-register (instruction word) and bits 3 through 7 of the P-register specifies any location in the sector in which the instruction being executed is located. $(Y)_{1-7}$ are loaded from $(P)_{1-7}$ and $(Y)_{8-16}$ are loaded from $(M)_{8-16}$.

Sector Bit Zero-Indexed. -- A 14-bit address specified by the sum of bits 8 through 16 of the M-register (instruction word) and bits 3 through 16 of the X-register can specify any location in memory. $(M)_{8-16}$ are added to $(X)_{1-16}$ and the result is loaded into $(Y)_{1-16}$.

Sector Bit One-Indexed. -- A 14-bit address specified by the sum of bits 3 through 7 of the P-register, bits 8 through 16 of the M-register, and bits 1 through 16 of the X-register can specify any location in memory. The resultant sum is loaded into the Y-register.

Indirect Addressing

The Y-register is loaded as described in Direct Addressing and the contents of the memory location specified by the Y-register are loaded into the M-register. This address can specify any location in memory. If M02 is a ZERO (no indexing), the contents of the M-register is loaded into the Y-register. If M02 is a ONE, the sum of $(M)_{1-16}$ and $(X)_{1-16}$ is loaded into the Y-register. When further indirect addressing is called for (M01 is a ONE), the steps described in this paragraph are repeated.

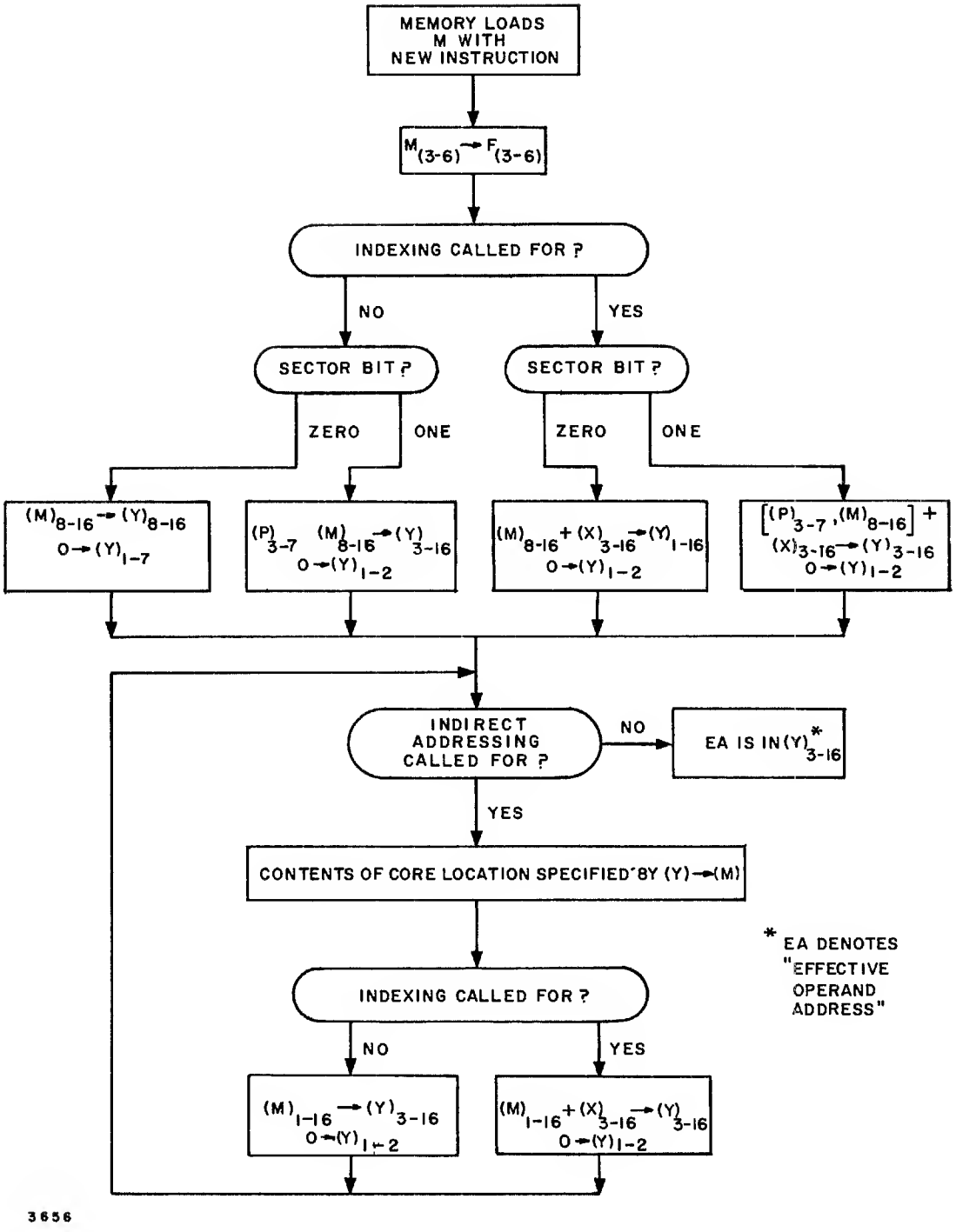


Figure 2-8. Memory Addressing Flow Chart

Instruction Execution Sequence

Program instruction processing (refer to Figure 2-9) requires from one to three types of machine phases. These phases are called F, A, and I. Instructions are composed of an integral number of phases, where each phase sets up the following one, depending on the instruction being performed.

Every instruction has an F phase. This phase fetches the instruction to be performed and performs indexing if the instruction word calls for indexing. If the instruction word calls for indirect addressing, the F phase sets up an I phase.

The I phase uses the address generated by the F phase to fetch a new address and performs indexing if the new address calls for indexing. If the new address calls another indirect address, an additional I phase is set up.

All memory reference instructions except JMP have at least one A phase. It is during an A phase that operands are fetched or stored and/or operated upon. When multiple or extended A phases are necessary, the shift counter is used.

The operand address used by the A phase is called the "effective operand address" (EA). It is established in the previous F or I phase. The last A phase sets up the F phase for the next instruction.

All instructions are composed of one of the nine phase sequences shown below:

F → F
F → I → F
F → I → I . . . → I → F
F → A → F
F → I → A → F
F → I → I . . . → I → A → F
F → A → A . . . → A → F
F → I → A → A . . . → A → F
F → I → I . . . → I → A → A . . . → A → F

The use of optional I/O devices can cause "breaks" and "interrupts" in the normal execution of a program in progress. A break is defined as an operation which interjects a function without altering the P-register. An interrupt is defined as an operation which interrupts the normal sequencing of instructions being performed by altering the P-register.

The computer breaks are RTC, MI, DMC, and DMA. RTC, MI, and DMC breaks can only occur when the CPU has completed an instruction. DMA can cause a break without waiting for the end of an instruction. SI and PI can interrupt only when the CPU is in the "permit interrupt" status. ML and PFI can interrupt regardless of the "permit interrupt" status.

Programs stored in memory can be executed at normal operating speed or may be examined in detail by executing one instruction at a time. Setting front panel controls for single instruction operation permits the first instruction, and every instruction thereafter, to be examined with front panel controls and indicators. Depressing the START button initiates the analysis. Thereafter, each time the START button is activated, the previously

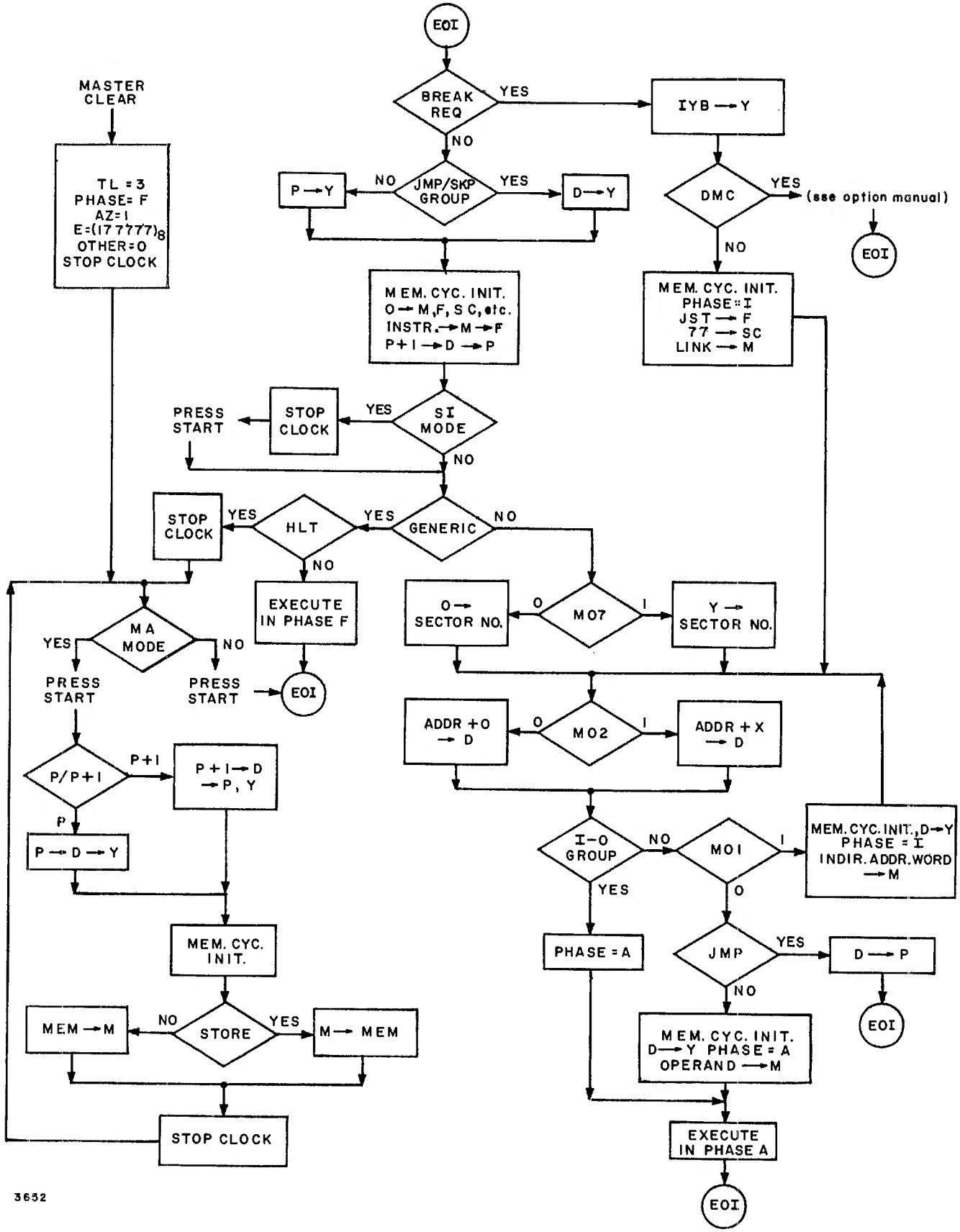


Figure 2-9. Basic Control Flow Chart

fetched instruction is executed and the next instruction is fetched. The Programmers Reference Manual, 3C Doc. No. 130071585, contains a discussion which treats this operation in greater detail.

When the operator desires to read and/or alter the content of any memory location, a memory access mode is initiated. Front panel controls and indicators permit the operator to display and alter the locations. Consecutive locations can also be displayed and/or altered with the proper selection of front panel controls.

CENTRAL PROCESSOR DATA FLOW

Figure 2-10 is a simplified diagram illustrating the flow of data to and through the central processor. The control logic is omitted for simplicity but is discussed in later text.

Note that the D-register is the central register through which most data flow occurs, hence its designation as the D (distribution) register. Entry into memory, buffered by the M-register, is possible either through the sum network to the D-register, or from the sum network directly to the M-register. The reader should become familiar with the mnemonics at the inputs to the registers. All signals with an E for the first letter are enable signals to route data from one functional area to another. For instance, EAS (an abbreviated form of EASTL) means "enable the A-register to the sum network", and EEA (an abbreviated form of EEALS/EEATS) means "enable the E-register to the A-register".

Other signals seen on Figure 2-10 are the SR/SL and the ENS signals. SRA, for instance, means "shift right to A-register." ENS means "enable the negation of the M-register to the sum network."

While still on the subject of the sum network, there are two other points worth mentioning at this time.

Note the input to the sum network with E1S16 and Y01 as inputs. This is used as a Compare A with Storage (CAS) instruction to skip one or two instructions based on the state of the Y01 bit.

The other point is the function of signals E1K17 and JAMKN as they pertain to the sum network. E1K17 is used to force a low-order carry and JAMKN is used to suppress all carries in the sum network.

The input bus has access to the central processor through the D-register. Control signal EID (enable input bus to D-register) gates the input bus information into the D-register. The output bus requires no such control signals to gain access to the contents of the A-register since it is always connected to the A-register.

FUNCTIONAL AREA DESCRIPTIONS

The following paragraphs contain descriptions of the column registers, the sum network (with examples of addition and subtraction), the clock system, the P-register, the shift counter, data transfers and operation decoding.

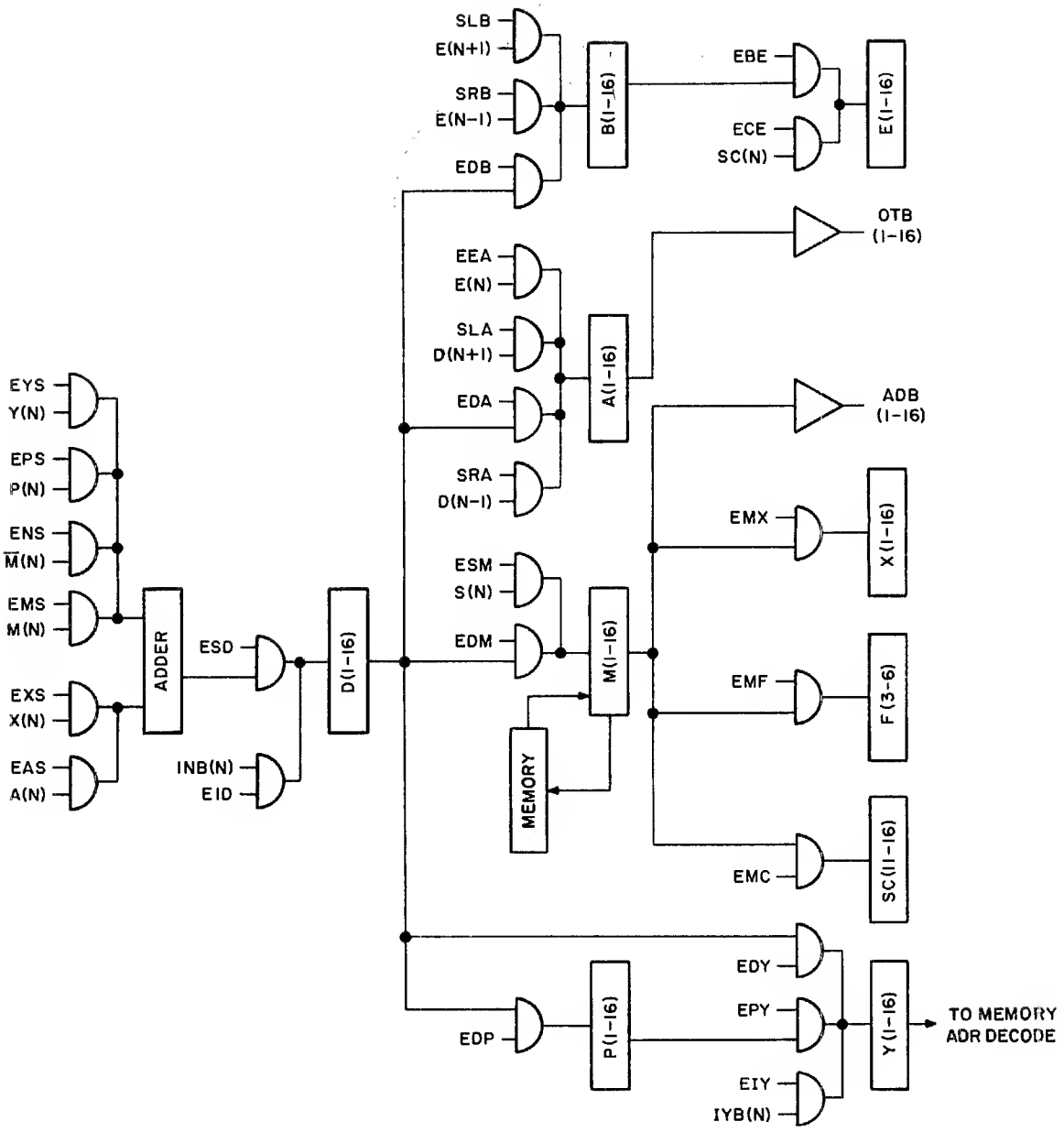


Figure 2-10. Control Processor Data Flow Chart

Column Registers

A-Register. -- The A-register is a 16-bit register used as the primary arithmetic and logic register of the computer. It can be displayed and manually controlled from the computer control panel.

B-Register. -- The B-register is a 16-bit secondary arithmetic register used to hold arithmetic operands which exceed one word in length. It can be displayed and manually controlled from the control panel.

P-Register. -- The P-register contains the location of the next instruction to be performed. Its contents are incremented by one each time an instruction is fetched and may be incremented an additional number of times during the execution of certain commands. In the case of a jump instruction the P-register is loaded with the memory location to which the program is to jump. During a Compare A with Storage instruction, the P-register can be caused to skip one or two instructions. The P-register can be manually controlled from the control panel.

Y-Register. -- The Y-register is a 16-bit memory address register. It can be displayed and manually controlled at the control panel.

E-Register. -- The E-register is a 16-bit register used when shifting the B-register.

D-Register. -- The D-register is a 16-bit register about which all local data flow in the central processor occurs. Transfers from the sum network to all other registers, except for the M-register which can be loaded directly from the sum network or the D-register, are made through the D-register.

F-Register. -- The F-register is a 4-bit register which copies and holds the Op Code contained in bits M03 through M06 of the M-register.

X-Register. -- The X-register is a 16-bit register used for address modification. Any memory cycle which alters the content of location zero also changes the X-register.

Sum Network

For purposes of this discussion, the sum network is to be considered as consisting of four parts; the summand selection, the intermediate functions, the carry network, and the sum formation/strobing networks. (See Figure 2-11.)

Summand Selection. -- With reference to Figure 2-12 and LBDs 101-116, note that there are two summands, G and H. Each of the summands is selected from among the several column registers (A or X for summand G and M, P or Y for summand H), depending on the algorithm of the current instruction. (See Figure 2-12.) Summand G can be gated from the A-register with enable level EASTL+ or from the X-register with enable level EXSTL+. If no selection is specified, the quiescent state of summand G is zero. Similarly, summand H

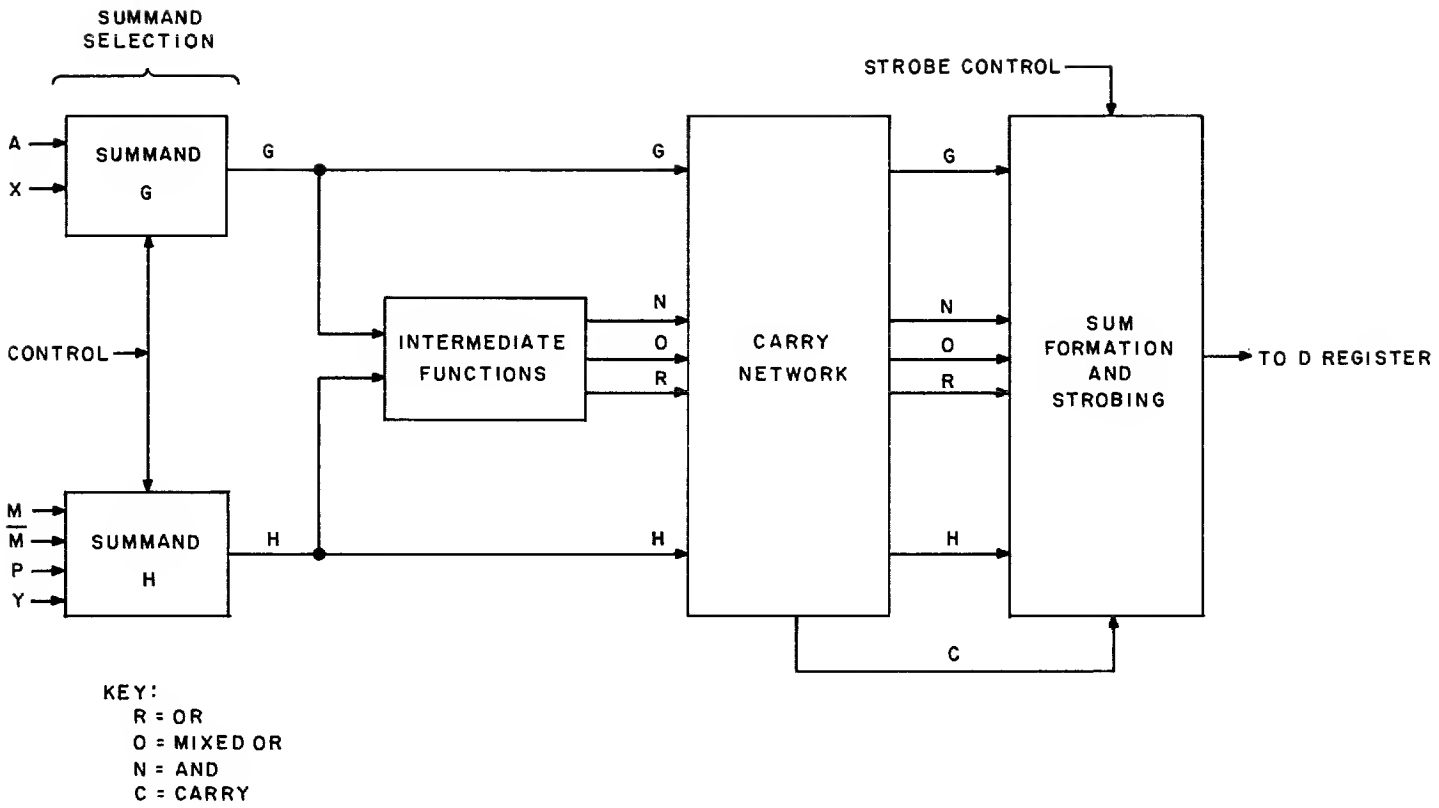


Figure 2-11. Sum Network Block Diagram

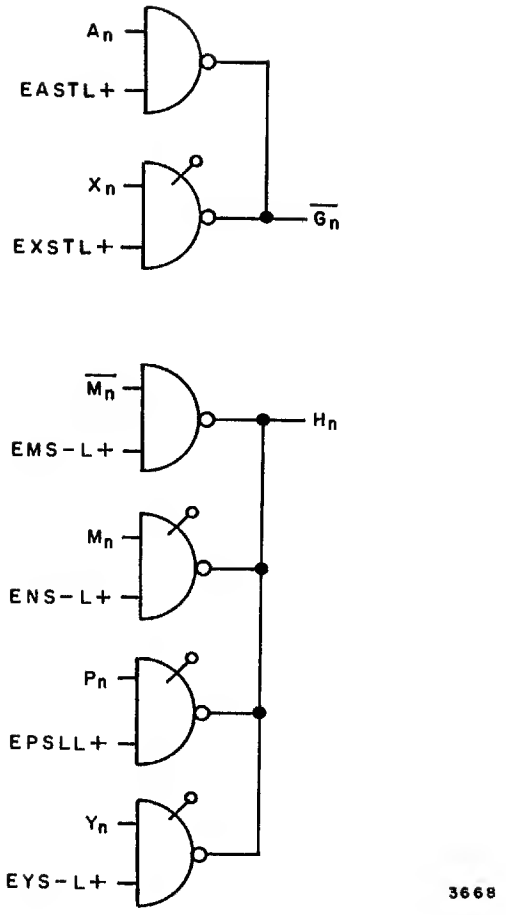


Figure 2-12. Summand Selection

can be gated from the M-register with enable levels EMSHL+ and EMSLL+, or from the one's complement of the M-register ($\overline{M}$) with ENSHL+ and ENSLL+, or from the P-register with EPSLL+, or from the Y-register with EYSHL+ and EYSLL+.

Note that the enable levels for selecting the M- and Y-registers are divided into a high and low order part to facilitate split word operations. The high order part of the input includes bits 1 through 7 and the low order part includes bits 8 through 16.

Since summand H is complemented relative to summand G (note polarities of inputs from registers on LBDs 101 through 116), the absence of any input to summand H renders it 177777_8 rather than zero. In some algorithms, more than one register can be simultaneously selected for the same bits of summand H. When this occurs, summand H becomes the logical product (AND) of the selected registers. If M and $\overline{M}$ are both selected, summand H becomes zero. This feature is used when data is merely transferred through the sum network with no arithmetic operations performed, as is the case in the interchange instructions and others.

Intermediate Functions. -- The intermediate functions comprise three high-speed gates per stage to produce the functions shown on Figure 2-13. These intermediate functions are used in the carry network and in the sum formation to be described. Rn is also used as a source of the assertion form of Gn, when summand H is equal to 177777_8, for the data path controlled by signal ESMTS+.

Carry Network. -- This network (see Figure 2-14 and LBD 117) is a succession of stages alternately forming the assertion and negation of the carry. The carry network implements the functions C_n and $\overline{C}_{n-1}$,

where: $C_n = (G_n + H_n)(G_n H_n + C_{n+1})$, and

$$\overline{C}_{n-1} = (\overline{G}_{n-1} + \overline{H}_{n-1})(\overline{G}_{n-1}\,\overline{H}_{n-1} + \overline{C}_n)$$

Note that the ripple carry propagation and the new carry generation signals are not combined, but are made available on two and sometimes three wires. The carry signal is required in negation form from every stage and in assertion form from at least one of any two adjacent stages. The inverters at the right of Figure 2-14 complete this requirement without adding to the ripple delay.

To achieve even faster settling in the carry network it is necessary to anticipate the ripple carry at selected stages. This process is described with the following equations:

$$C_7 = (G_7 + H_7)(G_7 \cdot H_7 + C_8)$$

$$C_6 = (G_6 + H_6)(G_6 \cdot H_6 + C_7)$$

$$C_5 = (G_5 + H_5)(G_5 \cdot H_5 + C_6)$$

$$= (G_5 + H_5)[G_5 \cdot H_5 + G_6 \cdot H_6 + (G_6 + H_6)G_7 \cdot H_7 + (G_6 + H_6)(G_7 + H_7)C_8]$$

A similar anticipation is applied in the generation of the carry from stages 12, 8, and 3, as shown on Figure 2-15.

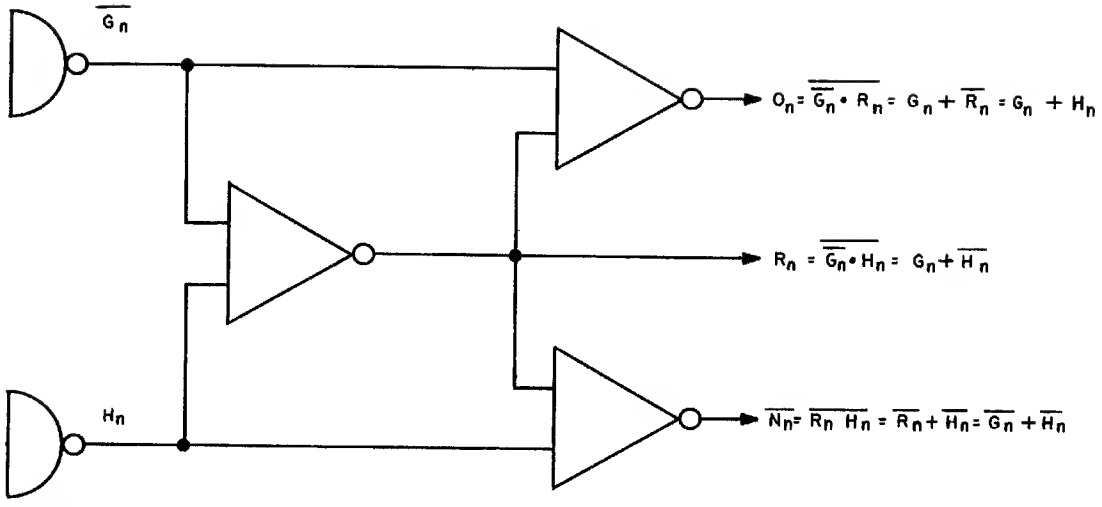


Figure 2-13. Intermediate Functions

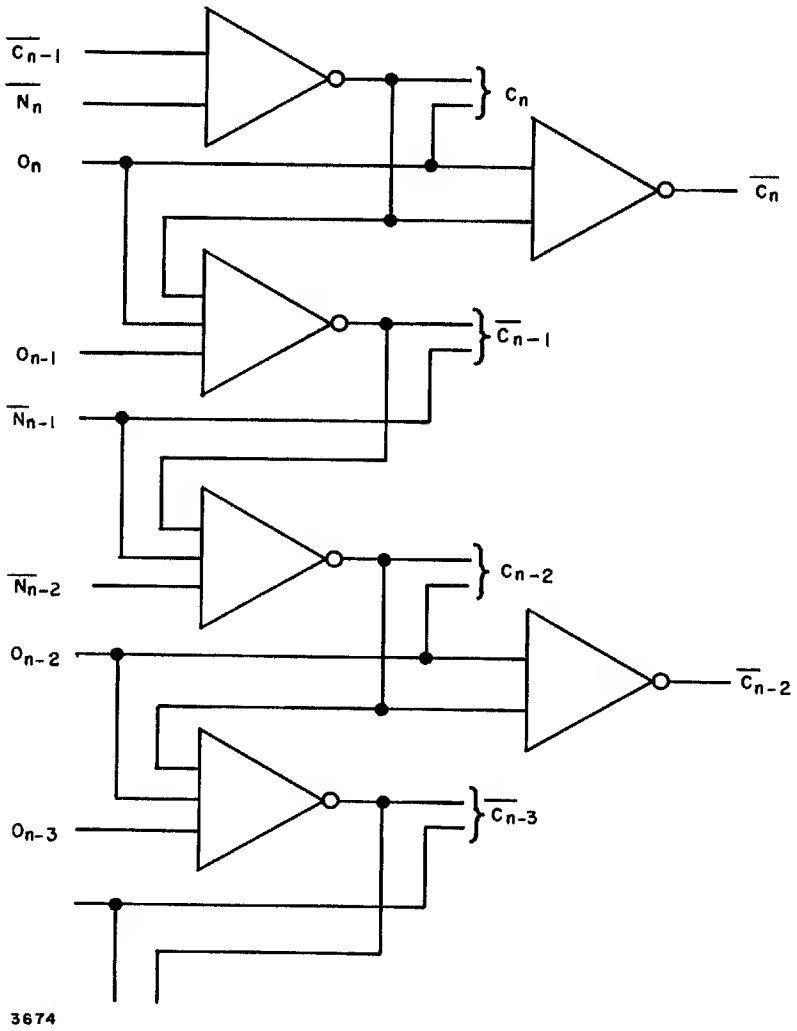


Figure 2-14. Carry Network Simplified Logic

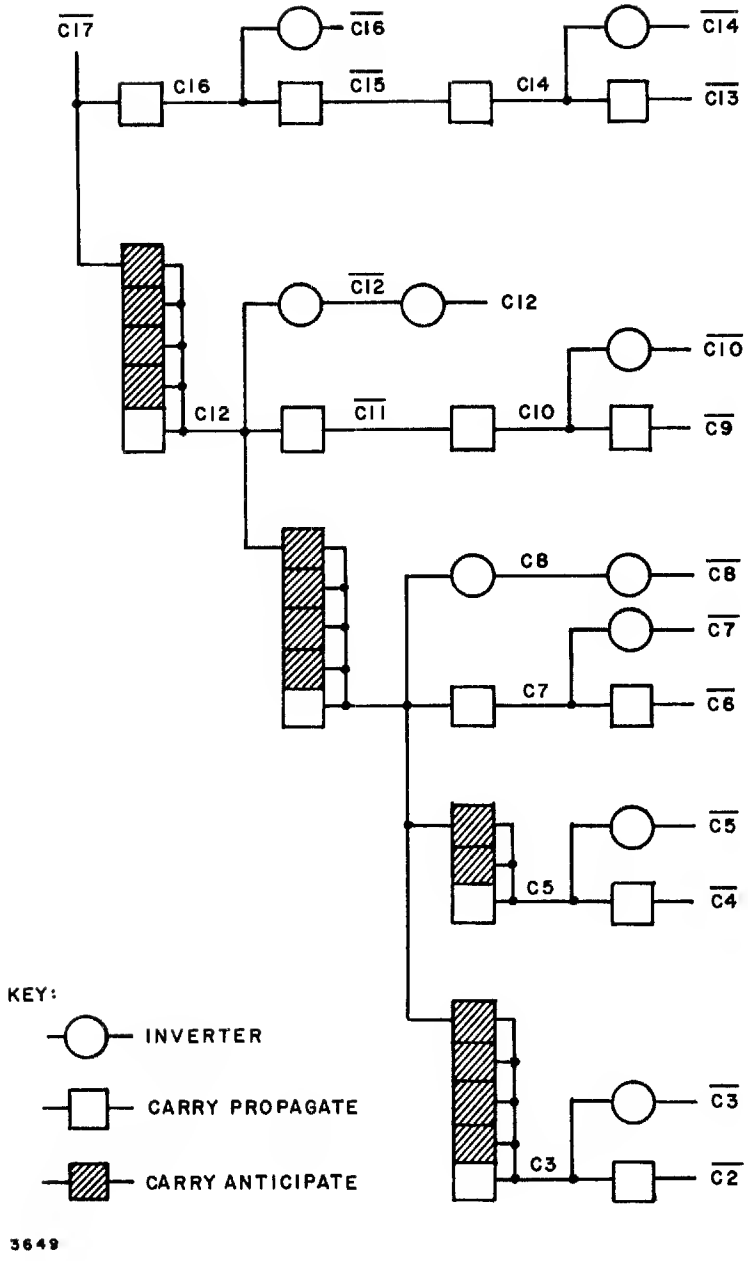


Figure 2-15. Carry Network Simplified Block Diagram

The least significant stage of the sum network (bit 16) provides for the injection of a ONE or a ZERO as a pseudo-carry from a non-existent 17th stage. This function (E1K17 from LBD 127) is used, for example, in the algorithm of the AOA (Add One to A) instruction. It is also widely used to offset the implicit -1 value which summand H assumes when no selection of registers M, P, or Y is specified. The same function also completes the two's complementing action required in the TCA, SUB, and CAS instructions.

During some algorithms (CMA, TCA, ERA) the sum network is used for forming the bit-by-bit exclusive-OR of summand G and summand H, rather than their algebraic sums. For this purpose signal JAMKN is applied to the intermediate function logic, the carry network and the sum formation gates. The effect of a ground on this line is to suppress all carries, (i.e., the output of each stage of the sum network is identical to that which would exist if the carry from the preceding stage was a logical ZERO).

Sum Formation and Strobing

The Boolean expression for the algebraic sum, S = G + H, can be manipulated into several equivalent forms:

$$S_n = \overline{G}_n \cdot \overline{H}_n \cdot C_{n+1} + \overline{G}_n \cdot H_n \cdot \overline{C}_{n+1} + G_n \cdot \overline{H}_n \cdot \overline{C}_{n+1} + G_n \cdot H_n \cdot C_{n+1}$$

$$\overline{S}_n = \overline{G}_n \cdot \overline{H}_n \cdot \overline{C}_{n+1} + \overline{G}_n \cdot H_n \cdot C_{n+1} + G_n \cdot \overline{H}_n \cdot C_{n+1} + G_n \cdot H_n \cdot \overline{C}_{n+1}$$

$$\overline{S}_n = \overline{G}_n (G_n + \overline{H}_n) \overline{C}_{n+1} + (G_n + H_n) (\overline{G}_n + \overline{H}_n) C_{n+1} + (G_n + \overline{H}_n) H_n \cdot \overline{C}_{n+1} \qquad (1)$$

Still another form of this expression is produced by noting, in the middle term of equation (1), that:

$$(\overline{G}_n + \overline{H}_n) C_n = (\overline{G}_n + \overline{H}_n) (G_n + H_n) (G_n \cdot H_n + C_{n+1}) =$$

$$(\overline{G}_n + \overline{H}_n) (G_n + H_n) C_{n+1}$$

Hence, $$\overline{S}_n = \overline{G}_n (G_n + \overline{H}_n) \overline{C}_{n+1} + (\overline{G}_n + \overline{H}_n) C_n + (G_n + \overline{H}_n) H_n \cdot \overline{C}_{n+1} \qquad (2)$$

Equation (1) is used in the sum logic (Figure 2-16) of those stages (15, 13, 11, 9, 7, 6, 4, 2) for which the carry from the previous stage is available in true form; equation (2) is implemented in the other stages.

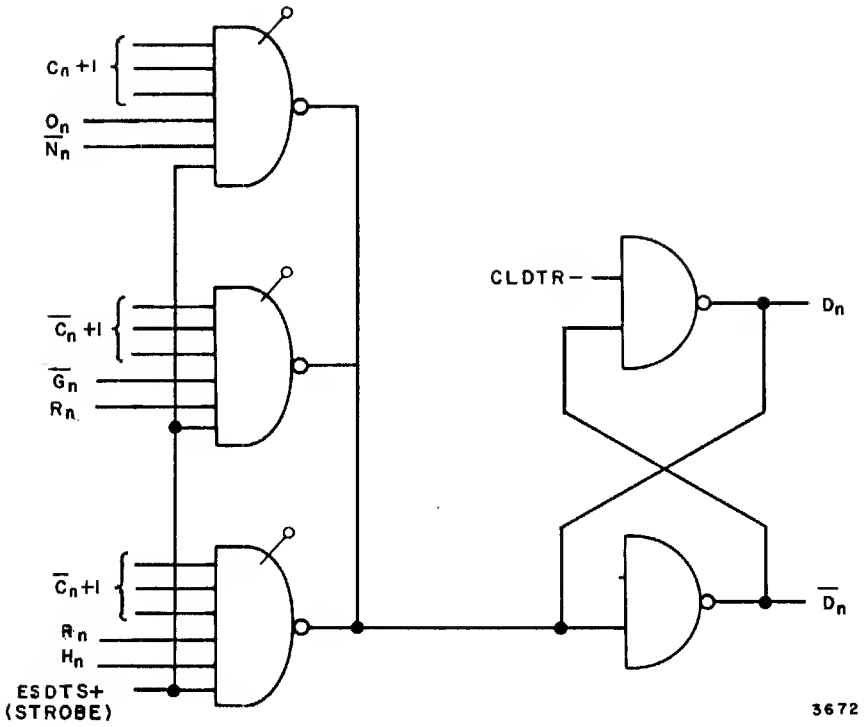


Figure 2-16. Sum Formation

To satisfy timing requirements, the sum logic for stage 1 is extended by a process analogous to the carry anticipation discussed in the preceding section:

$$\overline{S}_1 = \overline{G}_1 (G_1 + \overline{H}_1) \overline{C}_2 + (G_1 + H_1) (\overline{G}_1 + \overline{H}_1) C_2 + (G_1 + \overline{H}_1) H_1 \cdot \overline{C}_2$$

where $C_2 = (G_2 + H_2) (G_2 \cdot H_2 + C_3)$

therefore,

$$\overline{S}_1 = \overline{G}_1 (G_1 + \overline{H}_1) \overline{C}_2 + (G_1 + \overline{H}_1) H_1 \cdot \overline{C}_2 + (G_1 + H_1) (\overline{G}_1 + \overline{H}_1) G_2 \cdot H_2 +$$

$$(G_1 + H_1) (\overline{G}_1 + \overline{H}_1) (G_2 + H_2) C_3$$

$$\overline{S}_1 = \overline{G}_1 (G_1 + \overline{H}_1) \overline{C}_2 + (G_1 + \overline{H_1}) H_1 \cdot \overline{C}_2 + (G_1 + H_1) (\overline{G}_1 + \overline{H}_1) (G_2 + \overline{H}_2)$$

$$H_2 + (G_1 + H_1) (\overline{G}_1 + \overline{H}_1) (G_2 + H_2) C_3 \qquad (3)$$

This is the function implemented on LBD 101.

Another special case appears on LBD 130, where the extended-sign-bit, D_0, is created by combining the carry, C_1, with extended summand signs, G_1 and H_1:

$$\overline{S}_0 = \overline{G}_1 \cdot \overline{H}_1 \cdot \overline{C}_1 + \overline{G}_1 \cdot H_1 \cdot C_1 + G_1 \cdot \overline{H}_1 \cdot C_1 + G_1 \cdot H_1 \cdot \overline{C}_1$$

But, $C_1 = G_1 \cdot H_1 + (G_1 + H_1) C_2$

$$\overline{C}_1 = \overline{G}_1 \cdot \overline{H}_1 + (\overline{G}_1 + \overline{H}_1) \overline{C}_2$$

when $C_2 = (G_2 + H_2) (G_2 \cdot H_2 + C_3)$

Hence, $\overline{S}_0 = \overline{G}_1 \cdot \overline{H}_1 + \overline{G}_1 \cdot H_1 \cdot C_2 + G_1 \cdot \overline{H}_1 \cdot C_2$

$$= \overline{G}_1 \cdot \overline{H}_1 + (\overline{G}_1 + \overline{H}_1) C_2$$

$$= \overline{G}_1 (G_1 + \overline{H}_1) + (\overline{G}_1 + \overline{H}_1) (G_2 + H_2) (G_2 \cdot H_2 + C_3)$$

$$\overline{S}_0 = \overline{G}_1 (G_1 + \overline{H}_1) + (\overline{G}_1 + \overline{H}_1) (G_2 + \overline{H}_2) H_2 + (\overline{G}_1 + \overline{H}_1) (G_2 + H_2) C_3 \qquad (4)$$

Addition. -- This paragraph contains a discussion dealing with the addition of two positive numbers, a positive and a negative number, and two negative numbers. These examples represent the three different combinations encountered in addition.

Arithmetic operations in a two's complement oriented machine are logically easier to implement because the sign need not be considered, except to note overflow or underflow. The following examples show that in two's complement arithmetic, only binary additions

are required regardless of the sign of the data words.

For discussion purposes a 5-bit configuration is used (sign and 4 magnitude bits). The addition of two positive numbers is illustrated in Figure 2-17a. The contents of a memory location is stored in the M-register and added to the contents of the A-register. The addition occurs in the sum network. The sum of the two numbers is transferred to the A-register via the D-register.

The next case, a positive and a negative number is equally simple (Figure 2-17b). For this example the numbers +7 and -12 are to be added, the latter being in the A-register at the start of the addition.

All that needs to be done is to add A to the effective operand in memory (+7). The operand is transferred to the M-register and presented in summand H. The contents of A is presented to summand G. The sum is in two's complement (-5).

Adding two negative numbers is no more difficult since both numbers are in two's compliment. (Refer to Figure 2-17c.) The adding consists of presenting the contents of M to summand H (two's complement of -5) and presenting the contents of A to summand G (-9). The resultant sum is in two's complement (-14).

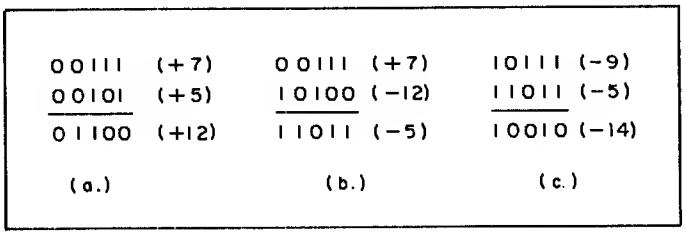


Figure 2-17. Addition Examples

Subtraction. -- Two's complement subtraction is quite simple (see Figure 2-18). One of the numbers (the contents of M) is two's complemented prior to being added to the contents of A. This occurs at the input of summand H with selection signals ENSHL and ENSLL, and carry injection sequal E1K17. The sum is transferred to D to provide the result directly to A.

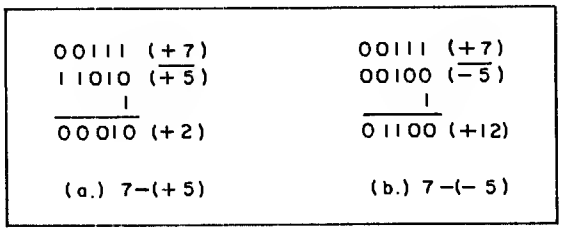


Figure 2-18. Subtraction Examples

Master Clock

All instructions in the central processor are performed sequentially and synchronously under the control of a two dimensional time grid. The two dimensions are fine and coarse. The fine dimension is controlled by the timing level generator (TLG). The coarse dimension is controlled by the phase-register which is discussed in later text.

At the heart of the time grid is the master clock oscillator (MCO). The MCO (LBD 118) generates three output waveforms, MCSET, MCRST, and MCTLG. The MCO is controlled by the start-stop logic (LBD 126) via the RUN flip-flop (RUNFF). When the computer is initialized, RUNFF is cleared and the MCO is at rest. Setting RUNFF starts the MCO through a five-epoch cycle. (See Table 2-1 and Figure 2-19.)

Table 2-1.
MCO Periods

Nominal Duration (ns)	MCSET	MCRST	MCTLG
120	0	0	0
15	1	1	0
75	1	1	1
15	1	0	1
15	1	0	0

The MCO continues to cycle until RUNFF is cleared with the MSTR CLEAR button on the control panel or with a programmed halt instruction (HLT). If the RUNFF is cleared during the MCRST pulse, no discontinuity is introduced into the MCO output waveforms. The MCO completes the cycle in progress and stops at the end of the fifth epoch (the trailing edge of MCSET).

Timing Levels. -- The timing level generator (TLG) controls the fine dimension of the timing grid (LBD 118). Normally, the system cycles sequentially through four timing levels; TL1FF, TL2FF, TL3FF, and TL4FF. Only one of these four levels is present at any time and the level changes at the end of each MCO cycle. When the system is initialized (see Figure 2-9), the TLG is preset such that only timing level 3 (TL3) is present. Auxiliary flip-flops TL13F, TL23F, and TL24F are set. When the MCO is started, each MCTLG pulse changes the auxiliary flip-flops in accordance with the current primary timing level. Thus, TL13F is set during TL1 and reset during TL3; TL23F is set during TL2 and reset during TL3; and TL24F is set during TL2 and reset during TL4. The states of the auxiliary flip-flops are then used (at the trailing edge of MCSET) to control the transition to the next timing level. (See Figure 2-20.)

During the execution of certain instructions (shifts, MPY, DIV, NRM, TCA, and HLT) the sequence of timing levels is modified. At these times the transition from TL3 to TL4 is blocked and the TLG returns to TL2. This is a function of signal RPTT2 (repeat TL2) (Figure 2-20 and 2-21).

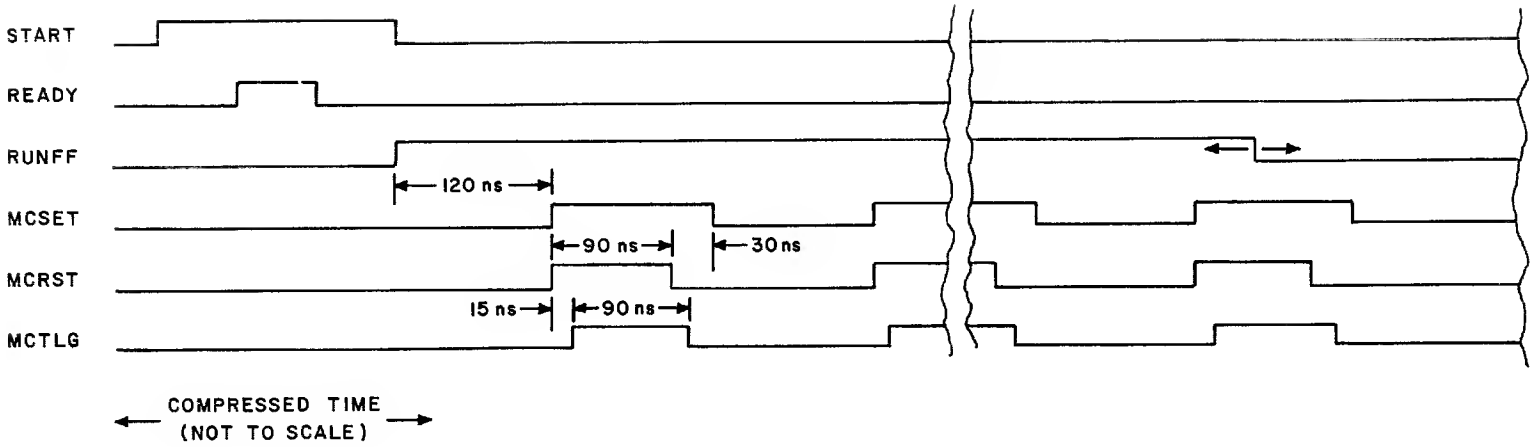


Figure 2-19. Master Clock Waveforms

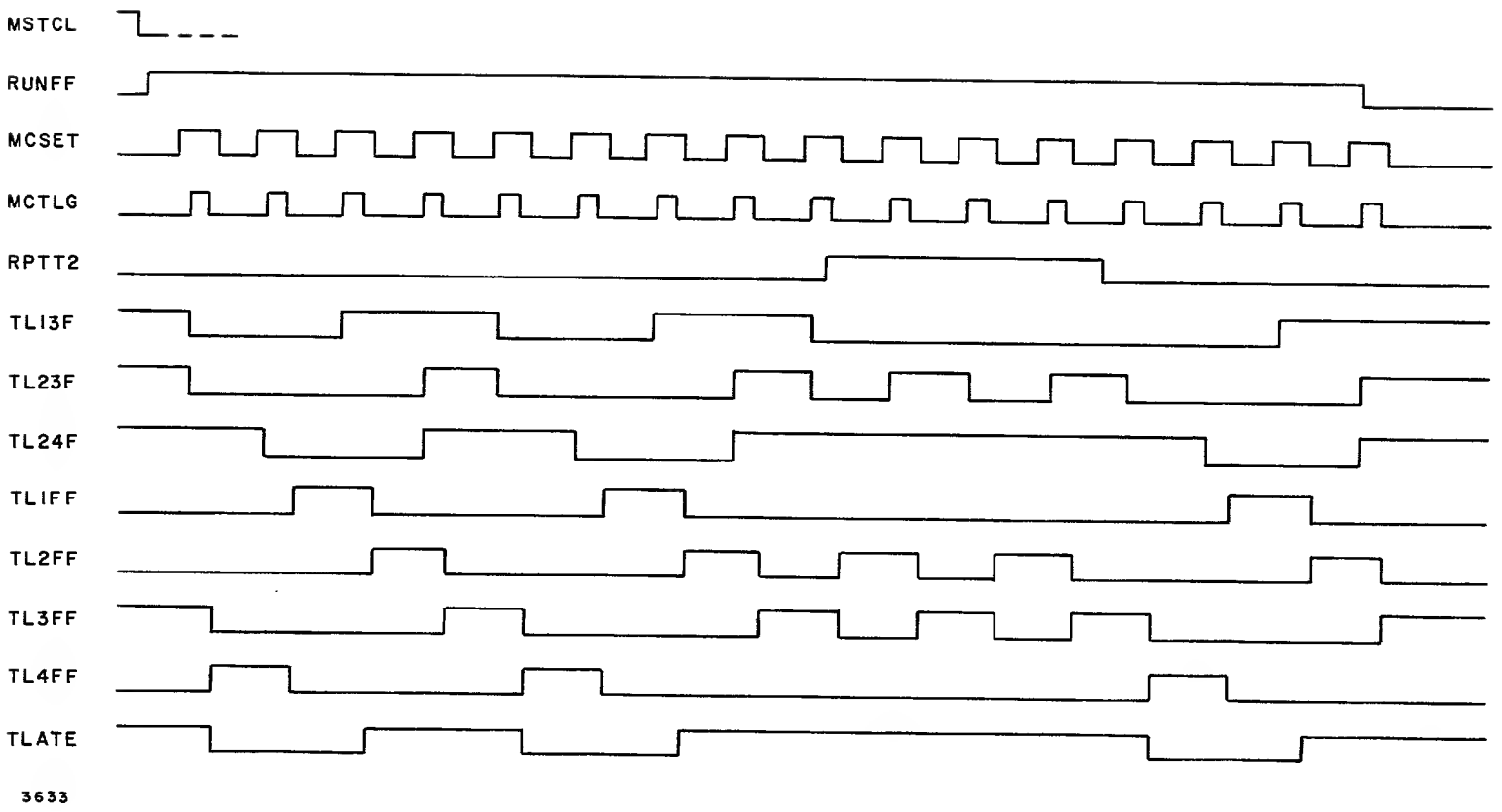


Figure 2-20. Master Clock Waveforms

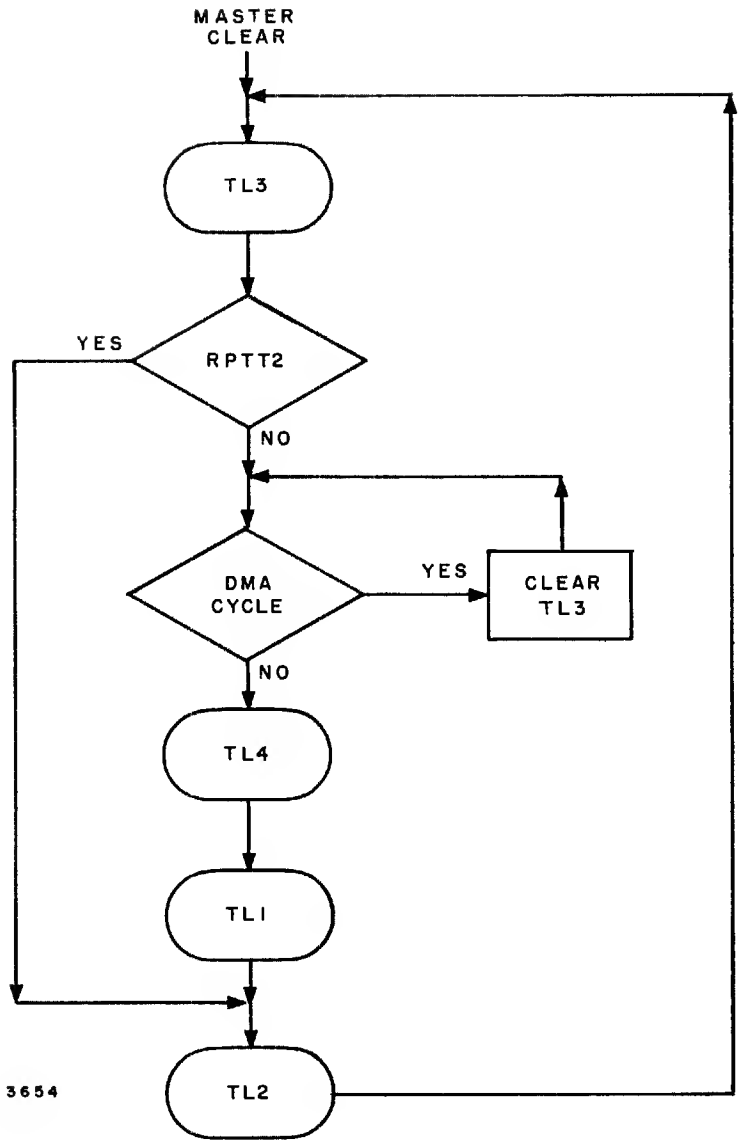


Figure 2-21. Timing Level Generator Flow Chart

The only other unusual action in the TLG operation occurs when the DMA option is installed and is actively servicing a device. The transition from TL3 to TL4 is blocked and TL3 is cleared. Note that this does not interfere with the RPTT2 action just described.

NOTE

Generally, options are not treated in this manual, however, an exception is made in this case to give a complete definition of the TLG function.

When the DMA cycle has been completed, TL4 is set and the TLG, and central processor in general, proceed as if no interruption had taken place.

Phase Register

The phase-register (LBD 119 and Figure 2-22) controls the second of two dimensions (coarse) of the timing grid described under the master clock. Three phases are sufficient for all central processor instruction sequences; the cycles are, Fetch (F), Indirect (I), and Execute (A). Each cycle starts with TL1 and ends with TL4. The duration of a phase is thus at least four clock cycles. It can be longer for the following reasons.

If signal RPTT2 is present, TL2 and TL3 are repeated for a total of at least six clock cycles (TL1, TL2, TL3, TL2, TL3, TL4). Certain A-cycle instructions are terminated with the second TL4 rather than the first TL4. This is a function of the contents of the shift counter. During the first pass through TL4, the shift counter does not equal zero; the A-cycle is terminated on the second pass when the shift counter is forced to zero. (See shift counter discussion.) The last example occurs during an indirect cycle when it is uninterrupted during multi-level indirect addressing.

Two versions of each phase are generated, an early and late cycle. For example, the F-cycle consists of FCYEF and FCYLF (F-cycle early and late, respectively). FCYEF is established during TL4 of the previous cycle, and is available for use in controlling actions during TL1 and TL2. FCYLF is copied from FCYEF during TL1 for use in controlling actions during TL3 and especially TL4. Some exceptions are made to these rules during TL2 and TL3 to equalize loading on the phase flip-flops.

Shift Counter

The shift counter (LBD 121) is a 6-bit counter which operates in conjunction with the phase-register to extend the execution of those instructions requiring more time. The F-cycle is extended for shift, TCA, and HLT instructions. The A-cycle is extended for JST, CAS, IRS, LDX, and others.

During TL1 of the fetch cycle of each central processor instruction, the shift counter is cleared to zero and remains in this state throughout the majority of operations. However, during the first TL3 of a shift instruction, for example, the shift counter is loaded from the instruction address field. This reflects the two's complement of the number of places to be shifted. At the end of TL3, the non-zero content of the shift counter enables the generation of control signal RPTT2 (repeat TL2) as previously described. TL2 is repeated as many times as is required to complete the designated number of shifts. Thus, the shift counter is responsible for determining the duration of the instruction (0.96 μsec plus 0.48 μsec per shift).

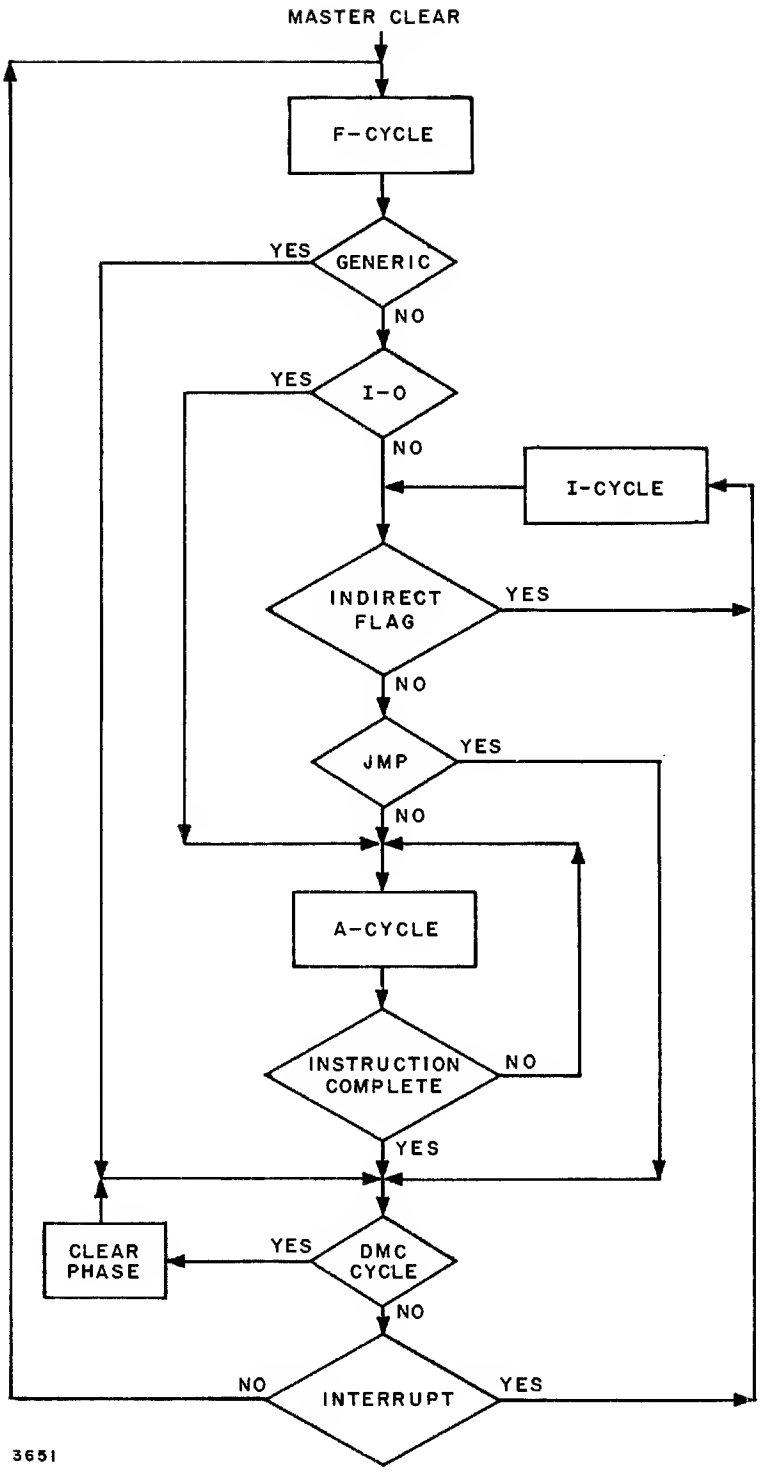


Figure 2-22. Phase Register Flow Chart

Data Storage

The various data storage registers in the central processor are formed with cross-coupled gates. With rare exceptions, all data transfers into these registers are performed by clearing all bits of the registers and then setting selected bits of the register to the desired state. (The D, E, and X registers are cleared by setting them to all ONEs.)

These two steps are actually carried out in overlapping fashion using the MCRST and MCSET master clock signals. Figure 2-23 is a simplified logic diagram of a typical data transfer depicting the control and timing of these paths. The numbers in parenthesis denote the latest times at which various key signals stabilize (measured in nanoseconds from the end of the previous MCO cycle). The clearing (MCRST) and setting (MCSET) signals reach the receiving register simultaneously. Proper operation is ensured by the earlier termination of MCRST, combined with the common collector connection of the set gate to the flip-flop. (See Figure 2-23.)

Operation Decoding

The output of the F-register is used at the input of two binary-to-octal decoders (LBD 120)to develop signals for the various Op Codes used in the central processor. The F-register is loaded from the M-register during an F-cycle. With reference to Table 2-2, note that bit F03 enables only one of the two decoders at a time. Bits F04, F05, and F06 determine the specific Op Code.

Table 2-2.
Op Code Decoding

Op Code	F03	F04	F05	F06	
IMAOP-	1	0	1	1	A1C27-A (LBD120)
IRSOP-	1	0	1	0	
CASOP-	1	0	0	1	
JSTOP-	1	0	0	0	
DIVOP-	1	1	1	1	
MPYOP-	1	1	1	0	
LSXOP-	1	1	0	1	
IOGRP-	1	1	0	0	
ANAOP-	0	0	1	1	A1C28-A (LBD 120)
LDAOP-	0	0	1	0	
JMPOP-	0	0	0	1	
OPG00-	0	0	0	0	
SUBOP-	0	1	1	1	
ADDOP-	0	1	1	0	
ERAOP-	0	1	0	1	
STAOP-	0	1	0	0	

Certain similar instructions are grouped for convenience in the DDP-516. These groups are:

a. OPG00
b. OPG3C
c. OPGAA
d. OPGDP
e. OPGJS
f. OPGMD
g. OPGNS
h. OPGSM
i. OPGWR

OPG00 instructions have zeros in bit position M03 through M06. OPG3C instructions are three cycle memory reference instructions. These include JST, IRS, CAS, IMA, LDX, and double-precision instructions. The OPGAA instructions are those memory reference instructions that utilize the A-register during an A-cycle (with some exceptions). These include LDA, ANA, ERA, ADD, SUB, and IMA. Instructions utilizing double-precision arithmetic operation fall into the OPGDP group. These are ADD, SUB, LDA, and STA. OPGJS are those that jump or skip such as the JMP, JST, IRS, and skip enabled instructions.

Instructions involved with negative sums belong to the OPGNS instructions. They are SUB, IRS, and CAS. Instruction CAS satisfies these conditions only when $(A)_1$ equals $(M)_1$.

STA, IMA, LDX, and STX belong to group OPGSM. This group deals with a sum to M-register control as its common point. A write read control group, OPGWR, includes instructions STA, IMA, LDX, STX, IRS, and JST.

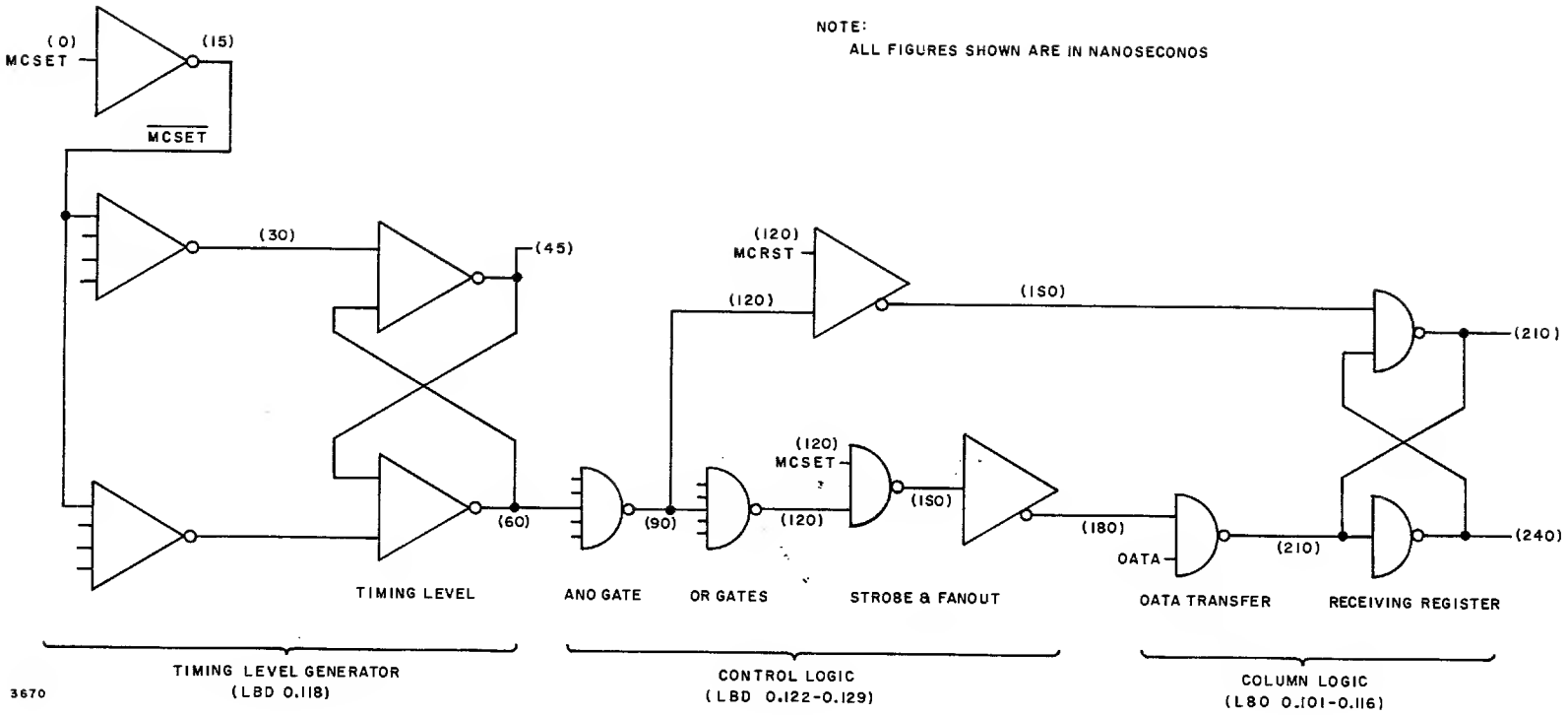


Figure 2-23. Clock Timing of Typical Data Transfer

SECTION 2. MEMORY SYSTEM

INTRODUCTION

This section contains a complete description of the memory system used in the DDP-516 computer. The following descriptive data is supplemented by the Function Index (Table 2-1) contained in Volume II, and by the logic and mechanical drawings contained in Volume III of these instructions. Descriptions of the μ-PAC integrated circuit modules used in the memory are contained in the Appendix.

MEMORY SYSTEM DESCRIPTION

The computer Magnetic Core Memory (see Figure 2-24) is a high-speed, digital storage device capable of storing a maximum of 16 bits (17 bits with parity option) of information in 4,096 or 8,192 randomly accessible locations. Maximum system memory capacity is 32,768 words and is determined by the complement of 4K and 8K memory modules in the system.

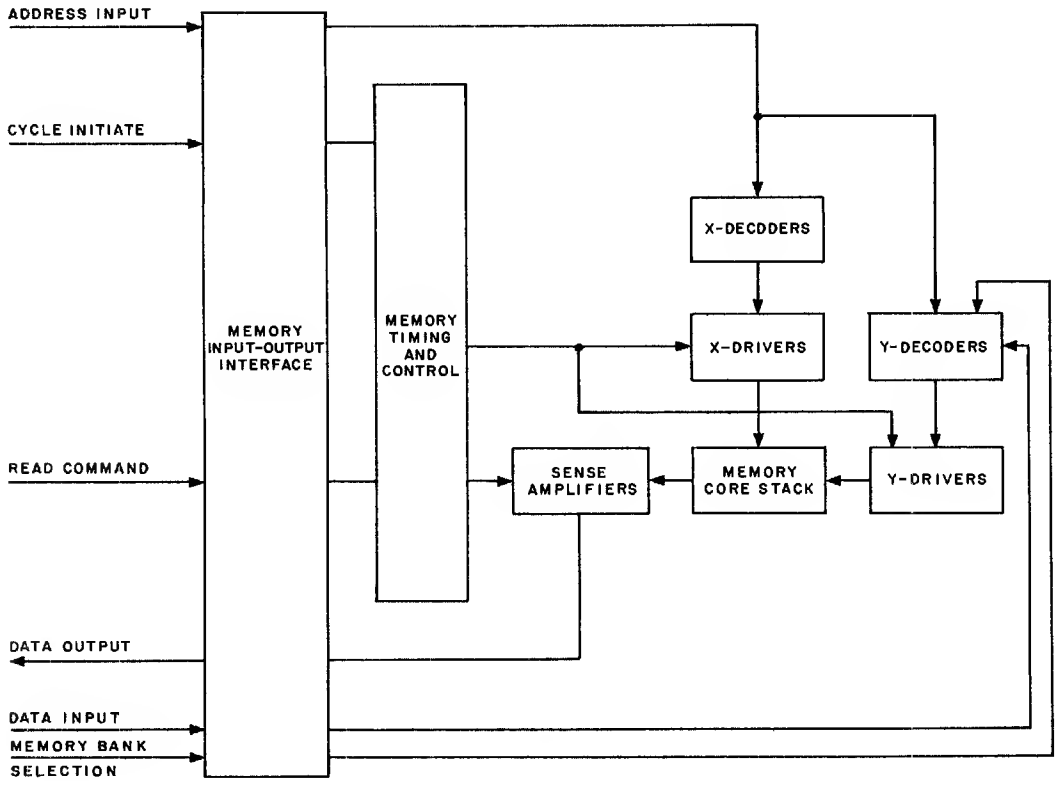


Figure 2-24. Memory Block Diagram

The memory is controlled by the computer and consists of the magnetic core array and associated control, timing, selection and sensing circuits. Data is stored in arrays of four 30 MIL OD by 18 MIL ID ferrite cores and selection is accomplished by three-wire, coincident-current techniques. Core switching time and frequency characteristics of the logic and driving circuitry contribute to a 0.96-μsec full cycle time and a 0.48-μsec access time. Data storage within the memory is both permanent and non-destructive. Exclusive use of monolithic circuitry and silicon conductors plus temperature compensation of drive currents with respect to stack temperature permits reliable operation between $0^{o}C$ to $50^{o}C$.

Memory address signals are received from the address bus at the beginning of any memory operation. The address inputs select the location of data stored within the core array. During a memory-load (clear-write) cycle, data to be stored is received from the computer M-register and, at the appropriate time in the cycle, data is transferred to the selected address in the memory core array. During a memory-unload (read-regenerate) cycle, the data word at the selected location is first transferred to the M-register and then regenerated (rewritten) into the core array.

A wide range of available memory capacities is made possible through the use of 4,096 and 8,192-word integrated circuit memory modules. The modules are designed to provide complete interchangeability and simplicity of storage expansion. Maximum storage capacity can be attained without sacrificing system performance capabilities.

MEMORY SYSTEM LAYOUT

The memory system is made up of as many as four independent memory modules, each of which is relocatable. To determine memory module location, reference should be made to the computer configuration drawing supplied as part of the documentation unique to the system since the location may vary from one system to another. Modules are mounted in the standard computer tilt-type drawers.

Each module consists of a mechanically coherent connector plane assembly, a core stack, necessary μ-PACs and a drive line terminating resistor plate assembly. The resistor plate assembly is permanently attached to the connector plane assembly by the resistor plate cable wiring.

LOGIC SIGNAL LIST

Logic signals used in the memory are identified and defined in the Functions Index contained in Volume II (Table 2-1) of this manual. Assertion signals (+6v true) are labeled "+" and negation signals (0v true) are labeled "-". Amplified signals have a letter following the polarity indicator (e.g., XXXXX+A).

MEMORY SPECIFICATIONS

Capacity:

32K, 24K, 16K, 12K, 8K or 4K randomly addressable 16-bit (or 17-bit) words.

Storage Mode:

Coincident-current magnetic core array (2-1/2 D, 3-wire)

Cycle Time:

0.96 μsec

Access Time:

0.48 μsec

Input/Output Levels

Passive: +6 volts

Active: GND

MEMORY CYCLE TIMING (See Figure 2-25)

For each memory cycle, the CPU must provide the memory with an address, a start signal and a read or write indication. Once the cycle has been initiated, another cannot be started until 0.96 μsec has elapsed.

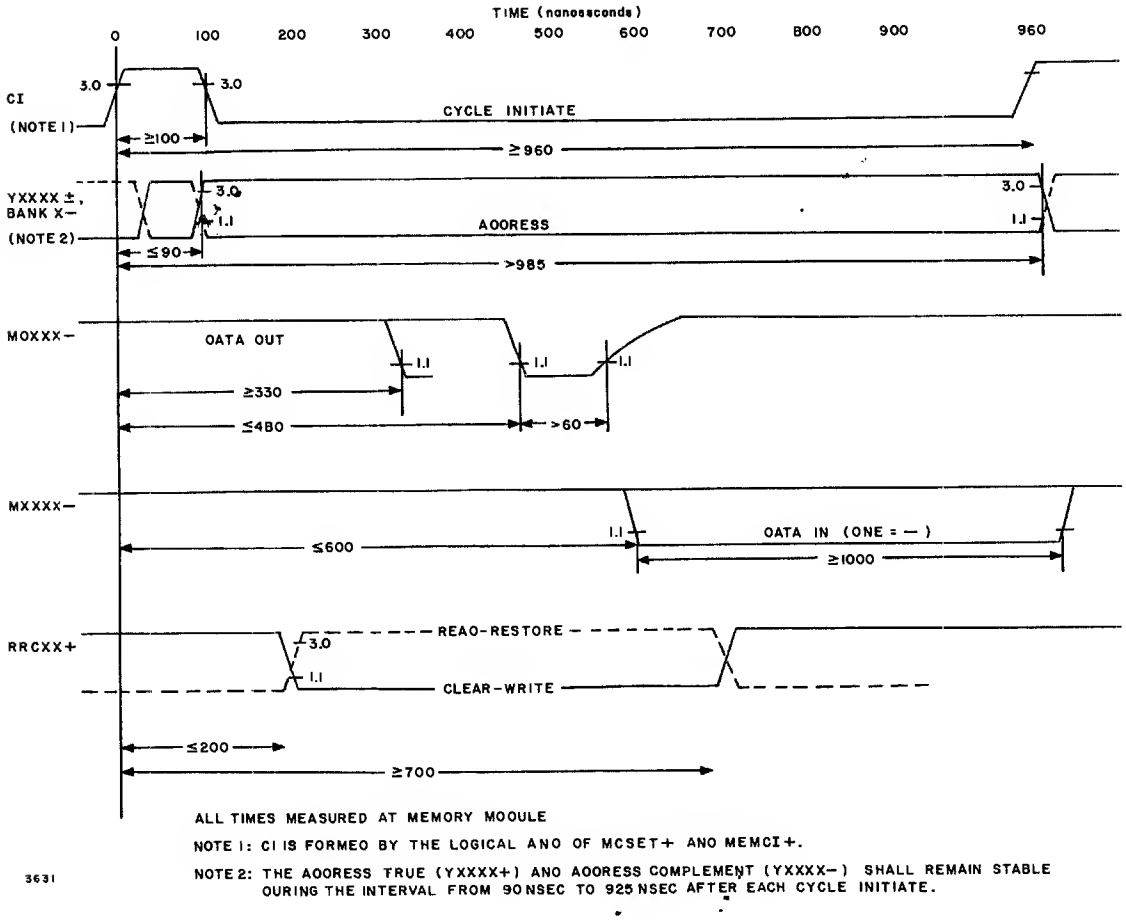


Figure 2-25. Interface Timing Requirements

During a read cycle, information will be available to the CPU no more than 0.48 μsec (access time) after the cycle is initiated. An additional 0.48 μsec is required for the memory to regenerate the information. If the memory is performing a write cycle, information must be made available to the memory within 0.60 μsec after cycle initiation.

INPUT/OUTPUT CABLE PIN ASSIGNMENTS

Table 2-3 lists I/O Cable Pin Assignments.

Table 2-3.
Memory Input-Output Cable Pin Assignments

Location C68 & B68		Location C67	Location C68 & B68		Location C67
Pin	Signal	Signal	Pin	Signal	Signal
1	Y16XX+	M01XX-	18	Y12XX-	MD02X-
2	Y15XX+	M02XX-	19	Y11XX-	MD03X-
3	Y14XX+	M03XX-	20	Y10XX-	MD04X-
4	Y13XX+	M04XX-	21	Y09XX-	MD05X-
5	Y12XX+	M05XX-	22	Y08XX-	MD06X-
6	Y11XX+	M06XX-	23	Y07XX-	MD07X-
7	Y10XX+	M07XX-	24	Y06XX-	MD08X-
8	Y09XX+	M08XX-	25	Y05XX-	MD09X-
9	Y08XX+	M09XX-	26	Y04XX-	MD10X-
10	Y07XX+	M10XX-	27	M15XX-	MD11X-
11	Y06XX+	M11XX-	28	MCSET+	MD12X-
12	Y05XX+	M12XX-	29	RRCXX+	MD13X-
13	Y04XX+	M13XX-	30	MEMCI	MD14X-
14	Y16XX-	M14XX-	31	M17XX-	MD15X-
15	Y15XX-	BANKX-	32	M16XX-	MD16X-
16	Y14XX-	MD17X-	33	GND	GND
17	Y13XX-	MD01X-	34	+6v	+6v

PRINCIPLES OF OPERATION

Storage Element

Information is stored in a three-dimensional array of 18 mil ID by 30 mil OD ferrite cores. Each core may be individually set to one of two possible magnetic states thereby representing one bit of binary information. Nonvolatile storage is made possible by core B-H characteristics which approximate a rectangular hysteresis loop. The core state is identified by the polarity of flux within the toroid structure. The switching mechanism may be qualitatively understood by examination of the B-H loop shown in Figure 2-26.

The H represents magnetizing force proportional to current magnitudes linking the toroid. The B symbolizes magnetic flux density within the core. The device characteristic

is useful since the B-H relationship is extremely nonlinear and irreversible. For example, if a core is initially in state 0, as magnetizing force is increased, B is slightly affected until H approaches H_1. As H increases from H_1 to H_2, total flux reversal occurs (path a). At H_2, the core may be considered saturated in the opposite state such that an additional increase in H cannot significantly alter B. Irreversibility is shown by the fact that, as H is relaxed from H_2 to 0, B returns to state 1 rather than starting point 0. However, state 0 can again be realized by applying sufficient H of opposite polarity to traverse path b.

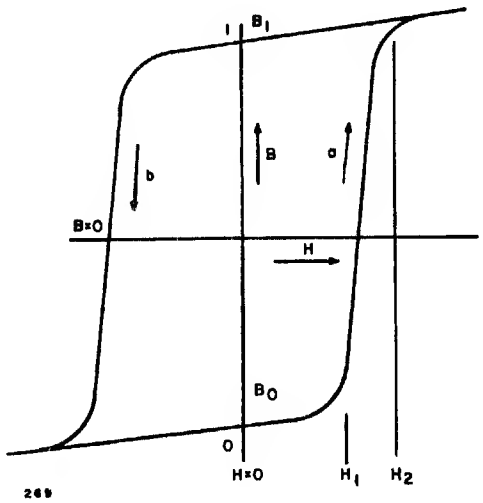


Figure 2-26. Typical B-H Characteristics

The threshold characteristic of the device allows its use in a coincident-current selection scheme such as that shown in Figure 2-27. Each core in the array is linked by an X- and Y- drive line. Subscripts R and W refer to read and write and + and - are polarity (direction) indicators. The current magnitude of IY or IX_R corresponds to H_1, or less, and their sum corresponds to a field exceeding H_2. Currents of this magnitude entering a core from the same side will produce a field exceeding H_2. Currents entering from opposite sides will have mutually cancelling fields resulting in H = 0. Currents IX_R and IX_W have the same amplitude but opposite polarity as do IY+ and IY-.

Each X- and Y- drive line links two cores in one bit array. The X- drive line is common to all bits. However, each bit has its own Y- drive lines. Prefixes 01 and 05 on the drive lines correspond to bits 1 and 5, respectively. Bits 1 and 5 are used in this example because they are physically located in the top and second planes in 4K and 8K memories.

If one X- drive line and one Y- drive line are energized, only one core in the entire array will see a magnetic field strong enough to cause it to change state. For example, if X1 and 01 Y1 are energized with IX_R and IY+, core $C_1$11+ will be switched to the ONE magnetic state (if not already in that state). $C_1$11- is subjected to a net field of zero and all other cores linked by 01Y1 and or X1 are subjected to half-currents. Consequently, a unique core address can be selected by energizing an X- drive line and one Y- drive line per bit.

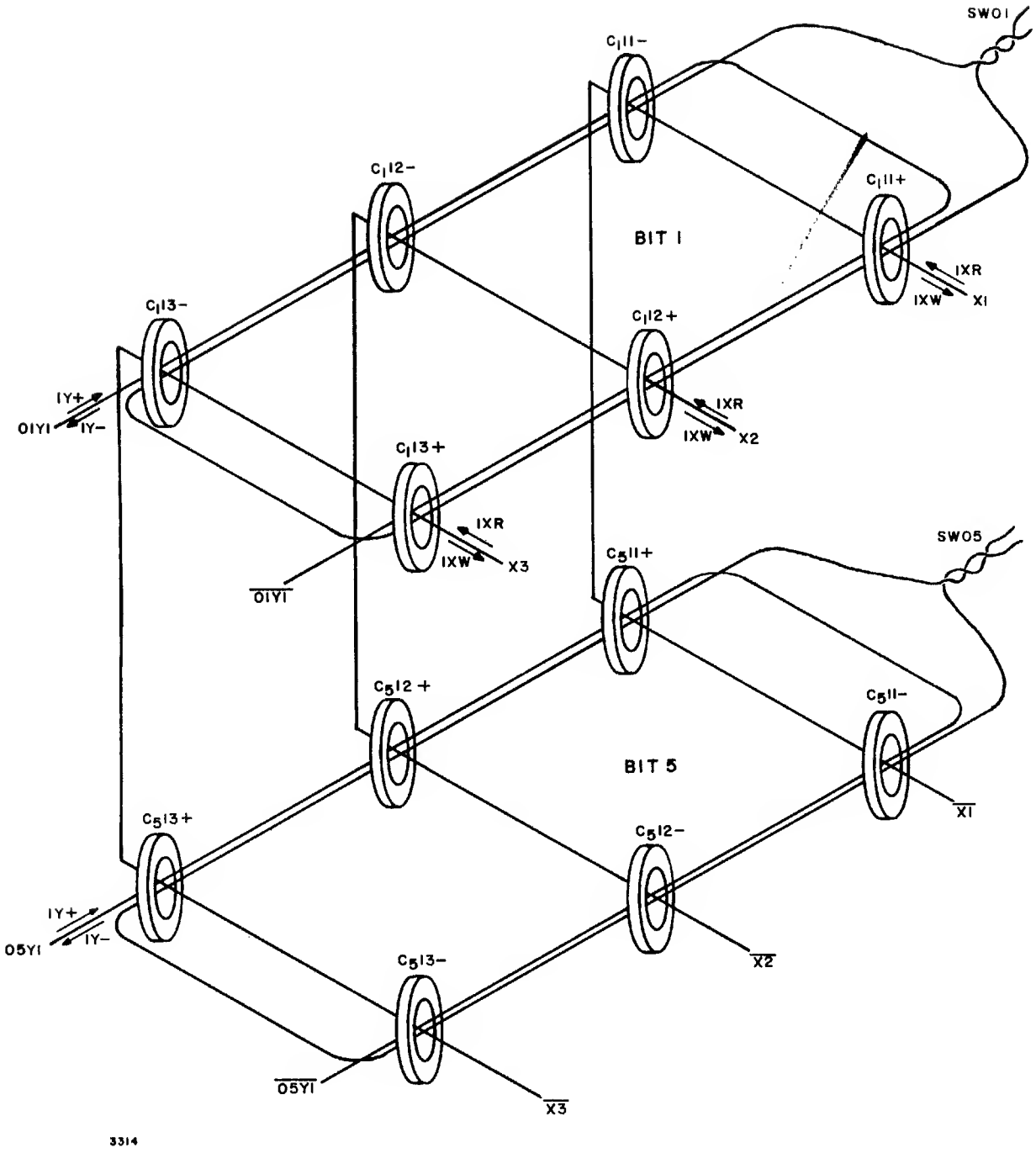


Figure 2-27. Coincident Current 2-1/2D Selection, Core Memory of 6 Words, 2 Bits

Consider a read operation with all cores in array one (bit 1) in the ONE magnetic state and all cores in array five (bit 5) in the ZERO state. Assume that IY+ drive currents flow in lines 01Y1 and 05Y1 and IX_R current flows in line X1. Core $C_1 11+$ is switched to the ZERO state and the resultant flux change appears as a differential voltage at the sense winding terminals (SW01). This voltage is amplified, strobed, and standardized,

setting the corresponding M-register stage to a ONE. If the direction of the Y- drive current is reversed (IY-), core $C_1$11- will be switched. Core $C_5$11+ was in the ZERO state so the currents drive the core further into saturation. This results in a flux change too small to be recognized by the sense amplifier. Core $C_5$11- is subjected to a net field of zero.

After the read operation, both cores at the selected address have been interrogated and the stored information has been transmitted to the central processor. Since the readout was destructive, the previously stored information must be reinserted during the write portion of the cycle. The M-register in the CPU presents the data to be restored in memory. This data, which is transmitted to the memory on lines MXXXX-, controls the Y- drive currents. Bit-1 currents flow, but there is no current in 05Y1 because the bit-5 data input is in the ZERO state. The result is that core $C_1$11+ is switched to the ONE and core $C_5$11+ remains in the ZERO state. All other cores remain in their original state.

ADDRESSING AND SELECTION

Address Inputs

Twenty-seven address lines control the memory selection circuits. These lines are described in the following paragraphs.

Thirteen address input lines (Y04XX+ through Y16XX+) provide the memory with the true binary coded address to be accessed. The address input complements (Y04XX- through Y16XX-) are also provided. One additional line (BANKX-) from the CPU will, when at 0 volt, select its associated memory module. When the BANKX- line attached to a given memory is at +6 volts, the digit drivers in that module are disabled. In addition, although the X-drivers turn on, and the timing is generated as in normal operation, core states within the module remain unchanged.

Decoding and Selection

A simplified diagram of address decoding and selection for a typical bit (bit 1) of an 8K memory is given in Figure 2-28. Each address line shown represents a binary bit. Four bits are transferred to the X- switches and four to the X- sinks. The X- switches uniquely enable one of 16 read/write output pairs going to the X- diode matrix. The X- sinks select one of 16 read/write buses, and the selected bus enables one of 16 drive lines. Only one of these drive lines is connected, at the opposite end, to an enabled diode matrix. Thus, only one of the 256 X- drive lines is selected.

Y-selection is accomplished in a manner similar to X- selection except that a read-write interchange is included. This operation constitutes changing the direction of read and write Y- currents with respect to X- currents. It is accomplished by making read and write timing inputs a function of Y10XX and results in less decoding circuitry being required. Selection of one of 32 effective Y- drive lines is made by selecting one of 16 wires. When Y10XX is a ZERO, the YSWRL+ and YSKRL+ signals are at +6 volts during the read portion

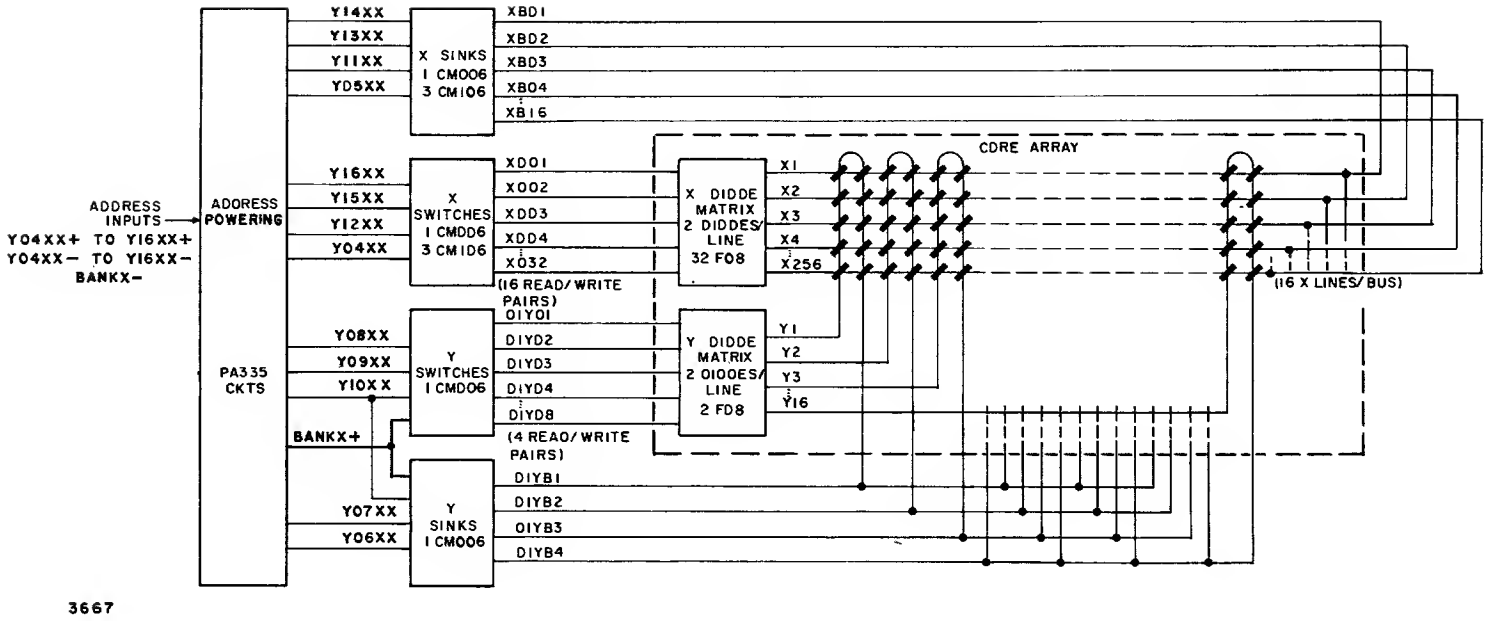


Figure 2-28. Address Decoding and Selection

of the cycle. Signals YSWRH+ and YSKRH+ are at +6 volts during the write portion. If Y10XX is a ONE, YSWRH+ and YSKRH+ are at +6 volts at read time and YSWRL+ and YSKRL+ are at +6 volts at write time. An X- drive line intersects with a Y- drive line at two cores, as shown in Figure 2-28. The relationship between X- and Y- currents (as controlled by Y10XX) defines which one of two cores is addressed.

The 4K decoding and selection method is similar to that described for 8K memories. The exception is that only 128 X- lines are selected in 4K memories.

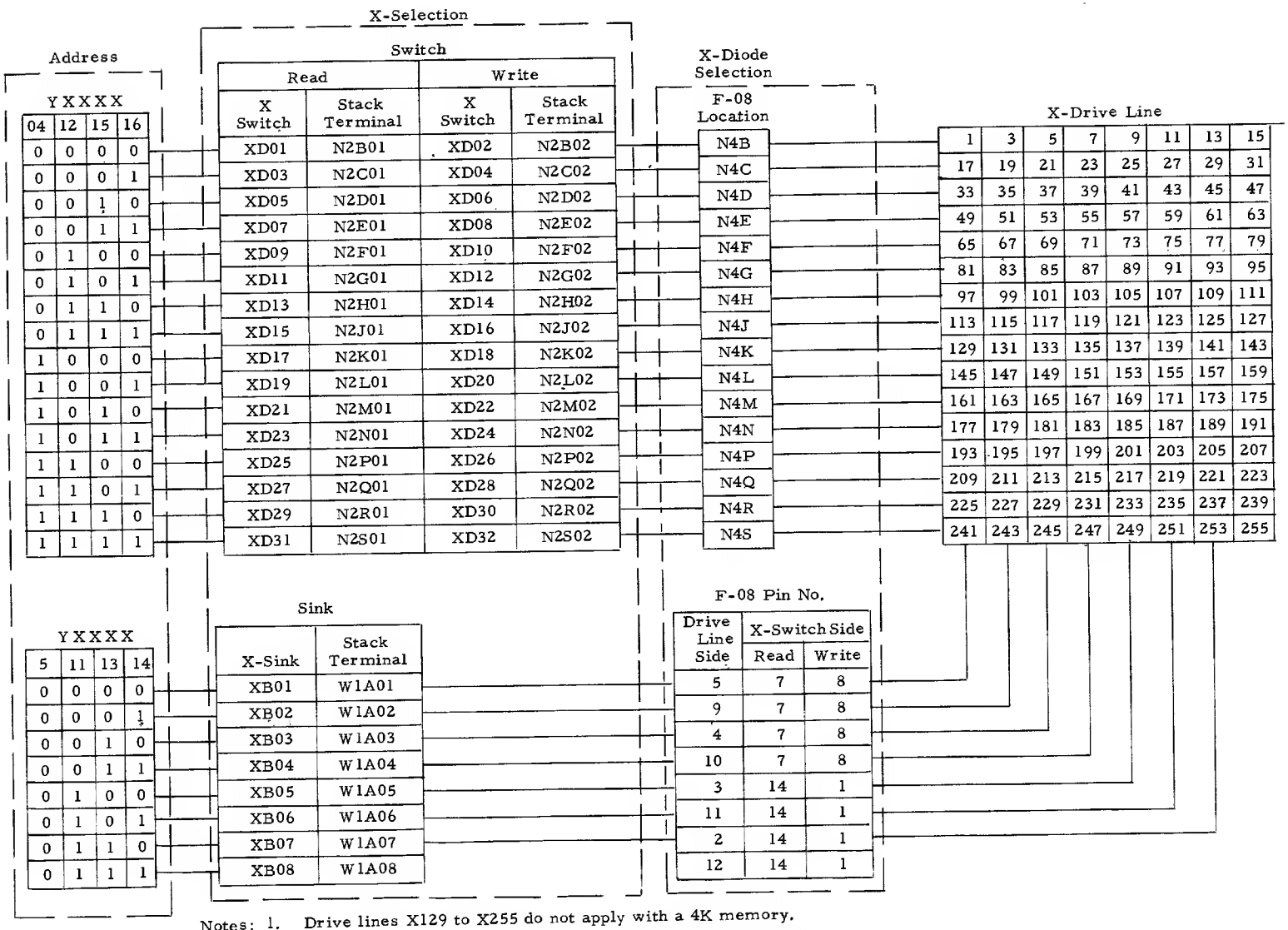
Address decoding and X- drive line selection for 8K memories is shown in Tables 2-4 and 2-5. Figure 2-30 is the X-selection schematic. The X- switch (XD01 through XD32), X- sink (XB01 through XB16), and X- drive line (X1 through X256) are shown selected by a given address. The X- selection for 4K memories is the same except that X- switch outputs XD17 through XD32 are not required. The stack location shown in the table refers to the location as shown on Figure 2-29. Referring to Table 2-4, assume address inputs 4, 12, 15, 16 are in the ONE state (+6 volts) and 5, 11, 13, 14 are in the ZERO state (0 volt). The read current path from switch XD31 to sink XB01, which selects drive line X241, is as follows: switch XD31, stack terminal N2S01, F-08 pin 7 at stack location N4S, F-08 pin 5 at stack location N4S, drive line X241, stack terminal W1A01, and sink XB01. The write current path for X241 is similar except for the selection of XD32 at terminal N2S02 and F-08 pin 8 at location N4S. Table 2-5 similarly depicts selection for even X- drive lines.

Address decoding and Y- drive line selection for both 4K and 8K memories is shown in Table 2-6. Figure 2-31 is the Y selection schematic. The terminal locations refer to the Y- switch and sink outputs to the Y- core plane. The stack connections (F-08 pin number, terminal, etc.) for a given bit can be determined from Table 2-6 and the Figure 2-29 bit location diagram. For example, read switch YD7 and sink YB3 are selected in bit 5 of an 8K memory by address Y05XX, Y06XX, Y07XX, Y08XX, Y09XX and Y10XX (010 110). The read current path from switch YD7 to sink YB3, which selects drive line Y17, is as follows: switch YD7, stack terminal Q1U01, F-08 pin 7 at stack location Q8, F-08 pin 9 at stack location Q8, drive line X17, stack terminal Q1T03, and sink YB3. The write current path for Y17 is similar except that YD8 is activated and the path is terminal Q1U05 and F-08 pin 8 at location Q8.

Figure 2-32 is a simplified diagram of the Y-selection electronics for one 8K bit. The selection switches are controlled by YSKRH+X and YSKRL+X. Enabling signals for the selection switches and sinks are ENYSW+X and ENSK1+X, respectively. The address inputs are decoded by the amplifier (PA) circuits. The MXXXX- input controls the Y- switches as a function of the input data during write time. The BANKX+X input is used to enable selection of Y- switches and sinks when the module is to be selected.

Assume that the address levels are decoded so that the ENSK1+X signal enables Y- sink power amplifier PA1 and that ENYSW+X has enabled a similar Y- switch amplifier. During the read portion of the cycle, YSKRL+X causes current to flow in the transformer associated with PA1. The secondary of the transformer turns on transistor Q4 and charging current flows to -V in drive lines Y1, Y3, Y4, Y2, Y9, Y11, Y12 and Y10 to -V.

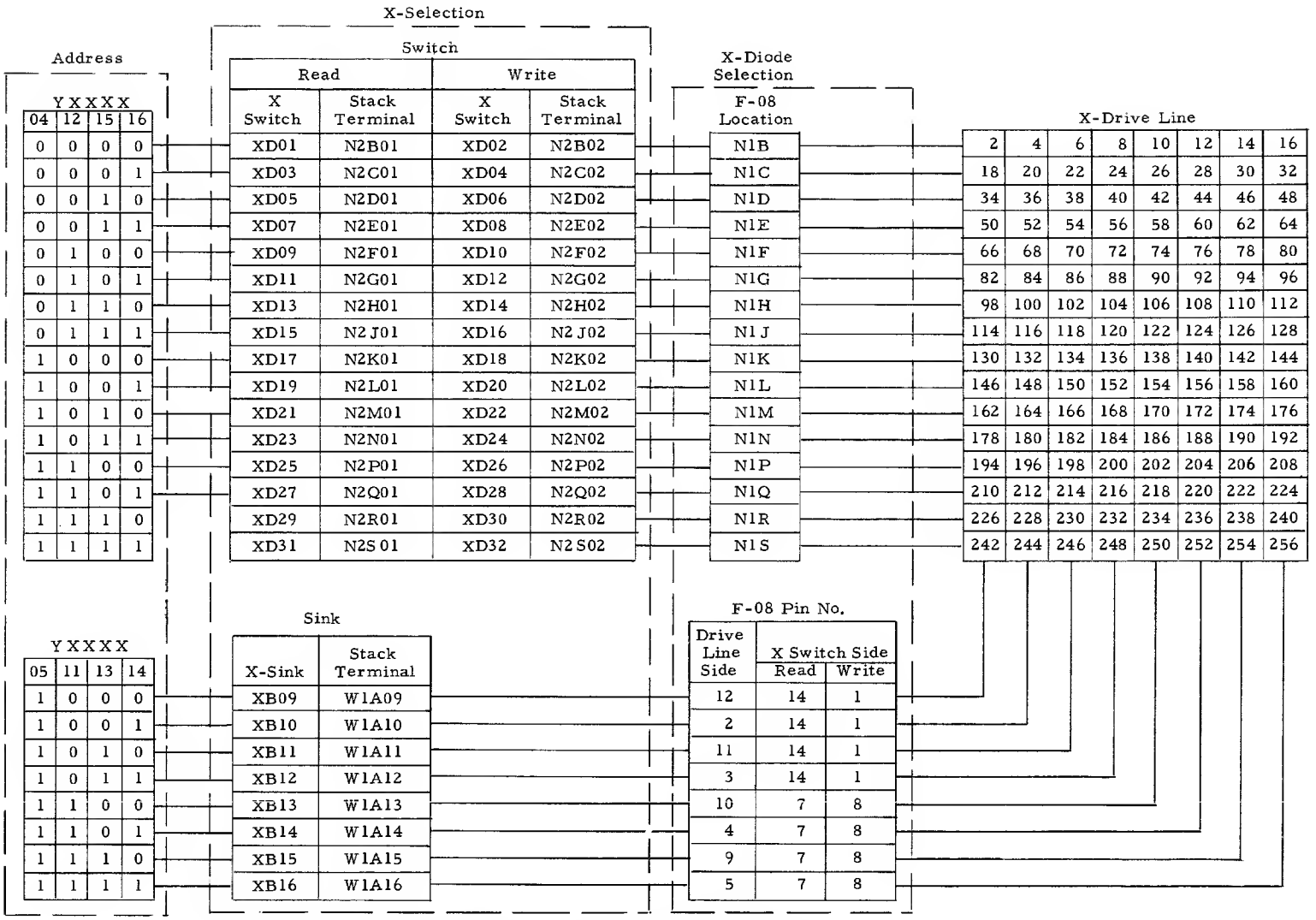
Table 2-4.
X-Decoding and Selection, Odd X-Drive Lines



Notes: 1. Drive lines X129 to X255 do not apply with a 4K memory.

2. If Y04XX is +6V in a selected 4096 memory module, the memory interrogation will be ignored. This should only result from a program error.

Table 2-5.
X-Decoding and Selection, Even X-Drive Lines



X-Selection

Address

Y X X X X			
04	12	15	16
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

Switch

Read		Write	
X Switch	Stack Terminal	X Switch	Stack Terminal
XD01	N2B01	XD02	N2B02
XD03	N2C01	XD04	N2C02
XD05	N2D01	XD06	N2D02
XD07	N2E01	XD08	N2E02
XD09	N2F01	XD10	N2F02
XD11	N2G01	XD12	N2G02
XD13	N2H01	XD14	N2H02
XD15	N2J01	XD16	N2J02
XD17	N2K01	XD18	N2K02
XD19	N2L01	XD20	N2L02
XD21	N2M01	XD22	N2M02
XD23	N2N01	XD24	N2N02
XD25	N2P01	XD26	N2P02
XD27	N2Q01	XD28	N2Q02
XD29	N2R01	XD30	N2R02
XD31	N2S01	XD32	N2S02

X-Diode Selection

F-08 Location
N1B
N1C
N1D
N1E
N1F
N1G
N1H
N1J
N1K
N1L
N1M
N1N
N1P
N1Q
N1R
N1S

X-Drive Line

2	4	6	8	10	12	14	16
18	20	22	24	26	28	30	32
34	36	38	40	42	44	46	48
50	52	54	56	58	60	62	64
66	68	70	72	74	76	78	80
82	84	86	88	90	92	94	96
98	100	102	104	106	108	110	112
114	116	118	120	122	124	126	128
130	132	134	136	138	140	142	144
146	148	150	152	154	156	158	160
162	164	166	168	170	172	174	176
178	180	182	184	186	188	190	192
194	196	198	200	202	204	206	208
210	212	214	216	218	220	222	224
226	228	230	232	234	236	238	240
242	244	246	248	250	252	254	256

Y X X X X			
05	11	13	14
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

Sink

X-Sink	Stack Terminal
XB09	W1A09
XB10	W1A10
XB11	W1A11
XB12	W1A12
XB13	W1A13
XB14	W1A14
XB15	W1A15
XB16	W1A16

F-08 Pin No.

Drive Line Side	X Switch Side	
	Read	Write
12	14	1
2	14	1
11	14	1
3	14	1
10	7	8
4	7	8
9	7	8
5	7	8

Notes: 1. Drive lines X130 to X256 do not apply with a 4K memory.

2. If Y04XX is +6V in a selected 4096 memory module, the memory interrogation will be ignored. This should only result from a program error.

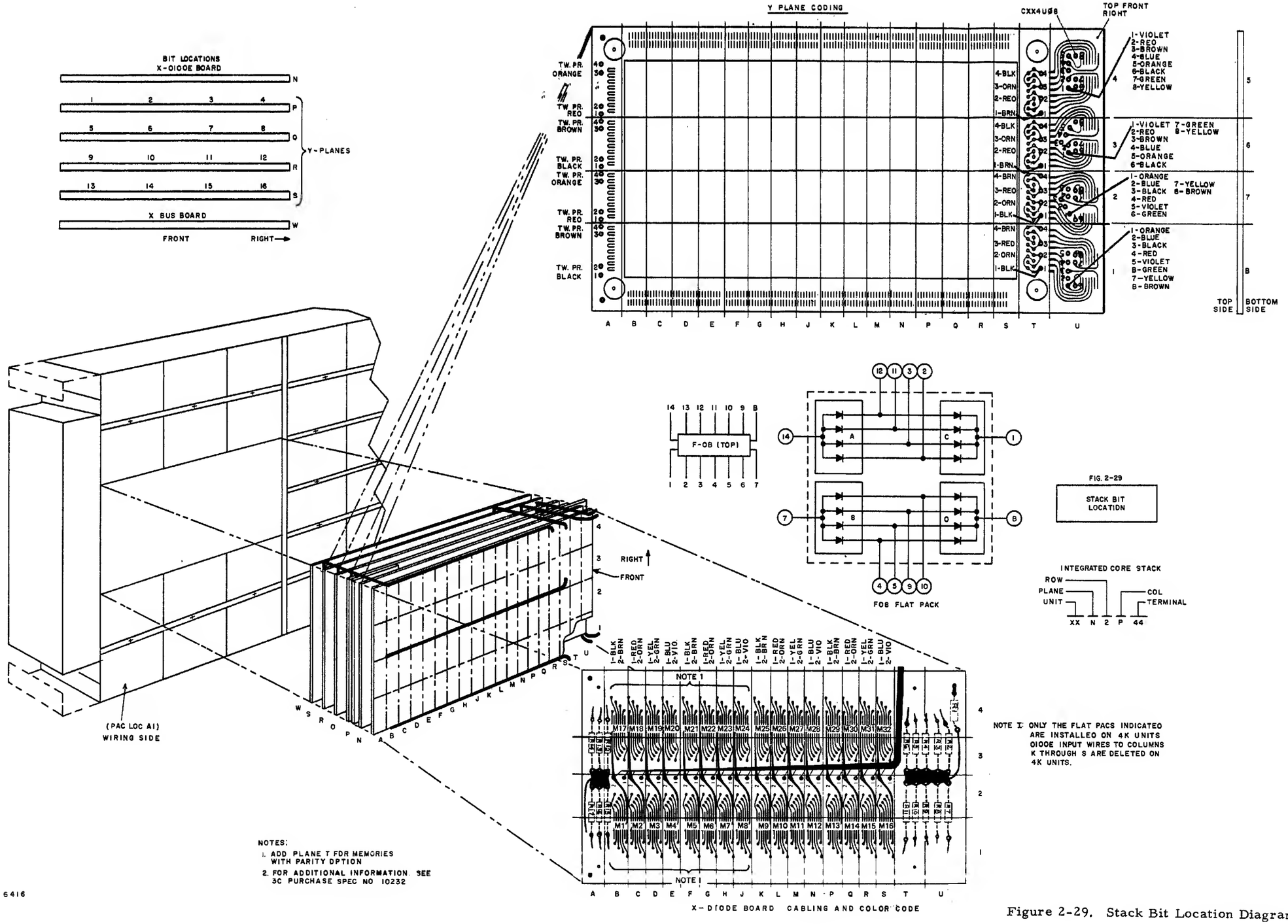
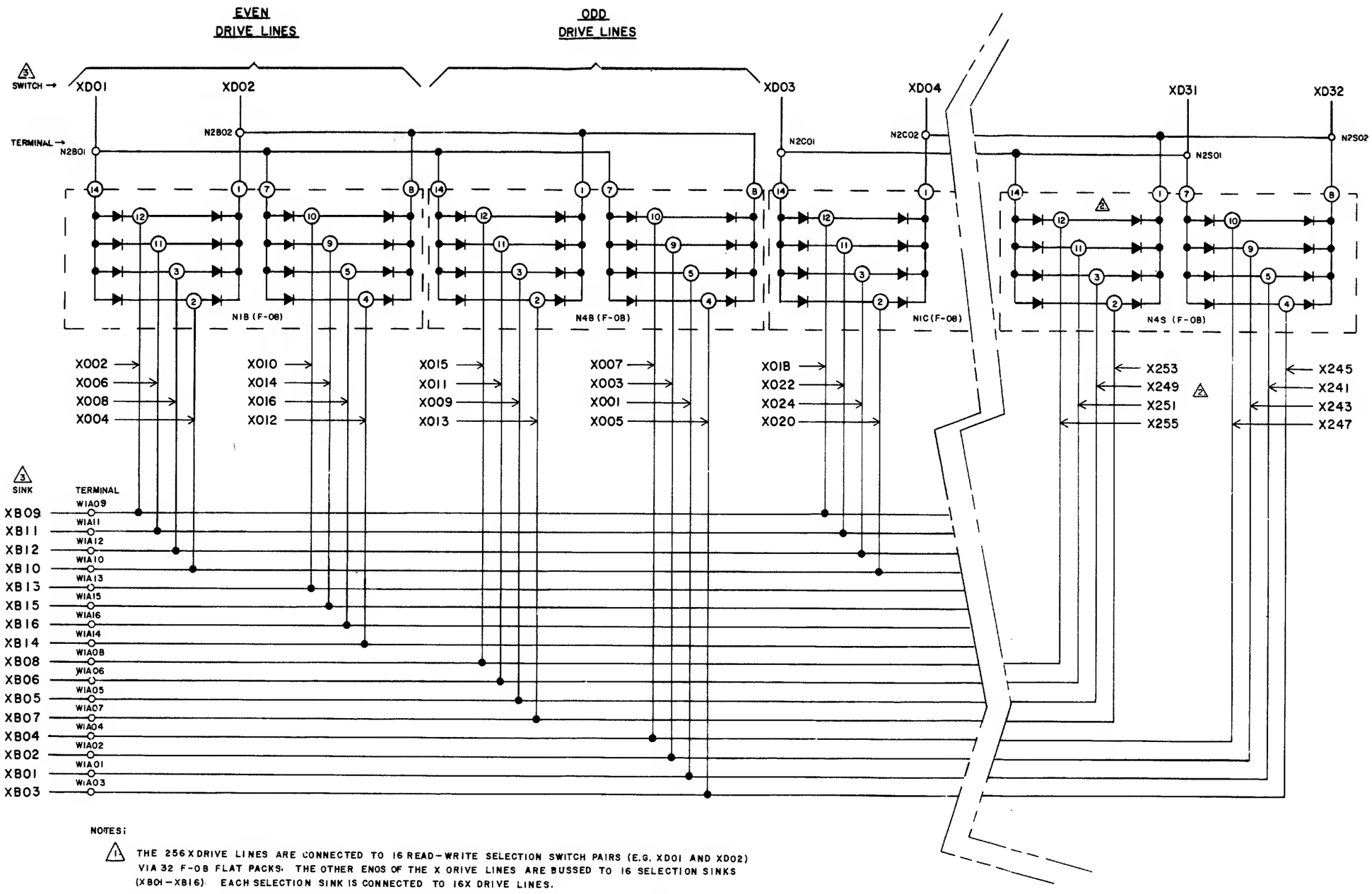


Figure 2-29. Stack Bit Location Diagram

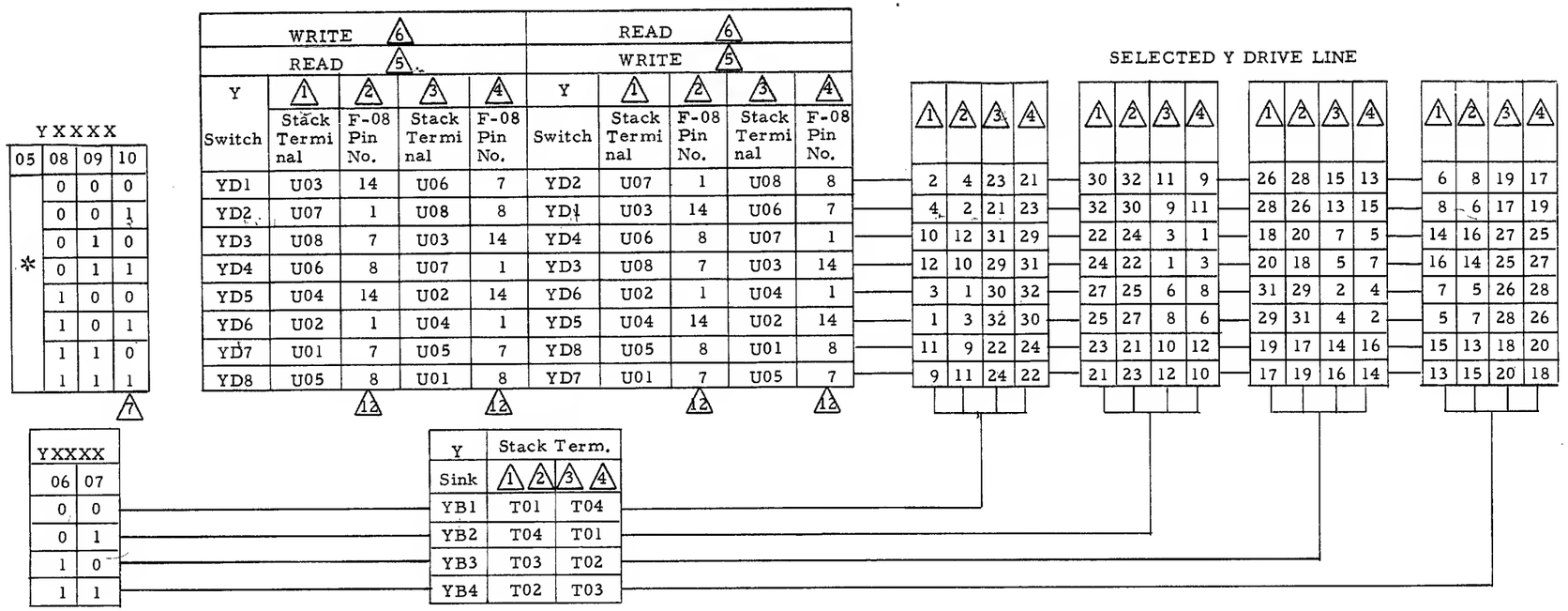


NOTES:

1. THE 256 X DRIVE LINES ARE CONNECTED TO 16 READ-WRITE SELECTION SWITCH PAIRS (E.G. XD01 AND XD02) VIA 32 F-08 FLAT PACKS. THE OTHER ENDS OF THE X DRIVE LINES ARE BUSSED TO 16 SELECTION SINKS (XB01-XB16). EACH SELECTION SINK IS CONNECTED TO 16 X DRIVE LINES.
2. ONLY 16 F-08 FLAT PACS ARE REQUIRED IN A 4K MEMORY (DRIVE LINES X129 TO X256 DO NOT APPLY).
3. SWITCH AND SINK INPUTS ARE FROM LBO 0.152.

Figure 2-30. Core Stack X-Selection Diagram

Table 2-6.
Y-Decoding and Selection



F-08 Location

BIT	Plane and Row Location		
	Stack Terminal	F-08	
	YB1-YB4 and YD1-YD8	YD1-YD4	YD5-YD8
1	P1	P1	P8
2	P2	P2	P7
3	P3	P6	P3
4	P4	P5	P4
5	Q1	Q1	Q8
6	Q2	Q2	Q7
7	Q3	Q6	Q3
8	Q4	Q5	Q4
9	R1	R1	R8
10	R2	R2	R7
11	R3	R6	R3
12	R4	R5	R4
13	S1	S1	S8
14	S2	S2	S7
15	S3	S6	S3
16	S4	S5	S4

5 6 5 6 5 6 5 6 5 6 5 6 5 6 5 6

* The selected branch of the end around Y line is dependent on X and Y current phasing. This alternates for odd and even bits, odd and even numbered planes, Y10XX and Y05XX.

*	Y05XX = logical 0	Y05XX = logical 1
1	Bits 1, 6, 9, 14	Bits 2, 5, 10, 13
2	Bits 2, 5, 10, 13	Bits 1, 6, 9, 14
3	Bits 3, 8, 11, 16	Bits 4, 7, 12, 15
4	Bits 4, 7, 12, 15	Bits 3, 8, 11, 16

The current polarity (read or write) varies as a function of the location of a bit on the plane. Refer to F08 location table for bits corresponding to the polarity shown in the Y decoding and selection table.

5 Y switch selection for odd numbered bits

6 Y switch selection for even numbered bits

7 Address AR07 is the interchange bit which reverses the phase of both switches and sinks. For decoding purposes it can be shown only with the switches.

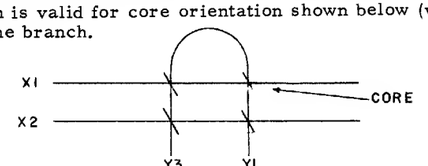
8 The "A" sense winding links Y lines
1, 2, 5, 6, 9, 10 13, 14, 17, 18, 21, 22, 25, 26, 29, and 30

The "B" sense winding links Y lines
3, 4, 7, 8, 11, 12, 15, 16, 19, 20, 23, 24, 27, 28, 31, and 32

9 For detailed information refer to the address register, regeneration loop and core stack Y selection logic diagrams.

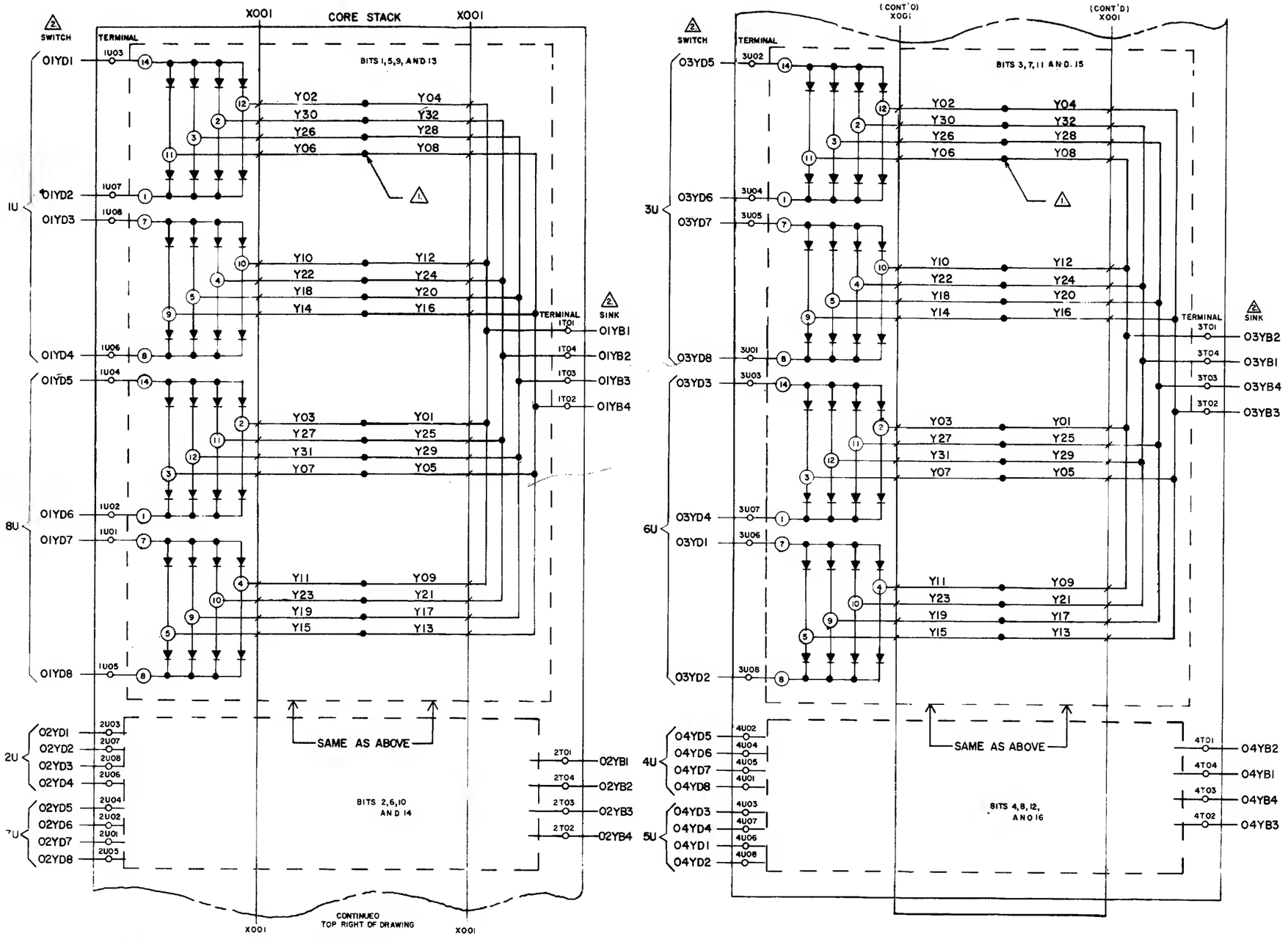
10 For memories with parity option use ICM-40 manual 130071411.

11 The selected Y line shown is valid for core orientation shown below (viewing core side of plane). Alternate orientation selects the alternate Y line branch.



12 F-08 pin numbers on the Y switch side. See Y Selection Schematic for F-08 pin numbers on the drive line side.

Table 2-6. Y-Decoding and Selection



1. Y DRIVE LINE TURN AROUND POINTS LOCATED IN ROW A OF THE Y CORE PLANES.
2. SWITCH AND SINK INPUTS ARE FROM L.S.O.'S 0,153- 0,160.

Figure 2-31. Core Stack Y-Selection Diagram

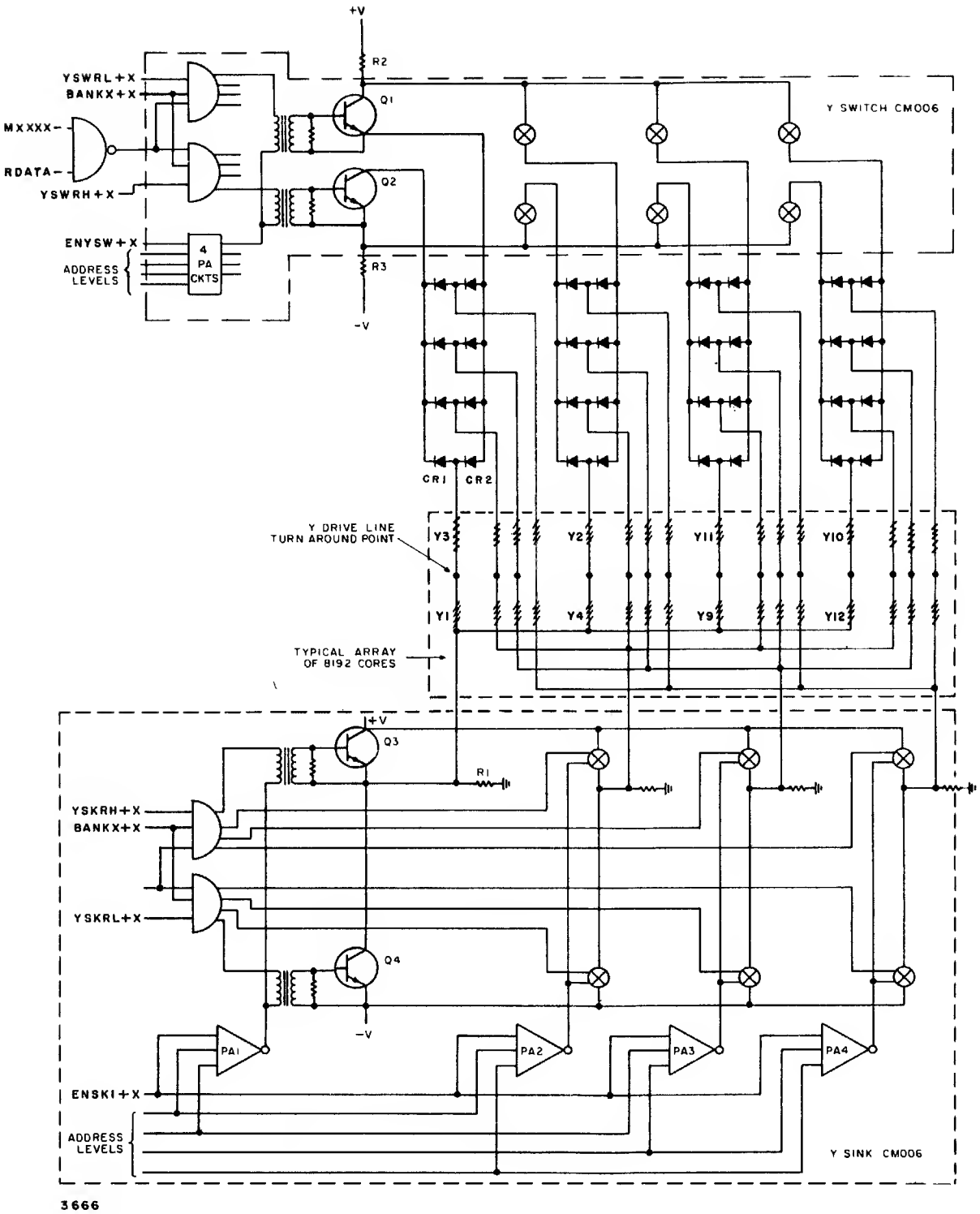


Figure 2-32. Simplified Decoding and Selection Matrix

Shortly after SKRW+X becomes +6 volts, YSWRL+ occurs and turns on Q1 (assuming BANKX+X is at +6 volts). Read current flows from +V, through R2, Q1, CR2, Y2, Y1 and Q4, to -V. Because of the orientation of the core array, only the core on the A half of drive line Y3 will switch. The output of the selected core is sensed and ultimately sets the data register to a ONE.

The address levels and enabling inputs (ENSK1+X and ENYSW+X) are the same during the write portion of the cycle. When the timing inputs (YSWRH+X and YSKRH+X) are generated, transistors Q2 and Q3 are turned on. This reverses the polarity of Y- drive current and write current flows from +V through Q3, Y1, Y3, CR1, Q2 and R3, to -V. The coincidence of X- and Y- drive currents results in the generation of a ONE in the selected core.

Write Y- drive current flows only if the data bit is at 0 volt. If a ZERO is to be written into the selected core, MXXXX will be at +6 volts and the Y- switch is prevented from turning on. The selected core receives only an X- write current so it remains in the ZERO state.

If Y10XX is in the ONE state, read current flows through R3, Q2, CR1, Y3, Y1 and Q3 and write current flows through R2, Q1, CR2, Y3, Y1 and Q4. This results in the selection of a core on drive line Y1.

The selection method shown in Figure 2-32 is used for X- and Y- selection in 4K and 8K memories. Y- selection is the same for both memories. However, 4K memories require fewer X- selection switches than 8K memories.

TIMING AND CONTROL

The logical functions associated with the control and distribution of memory functions are shown in the logic diagrams. Timing diagram for the standard memory is shown in LBD No. 162 of Volume III.

Operating Modes

Since the DDP-516 memory does not contain registers, operation in the clear-write mode is almost identical to that of the read-restore mode. The exception is that during clear-write operation, the read-restore command (RRCXX+) is at 0 volt and the sense amplifier strobe is disabled. When the strobe is disabled, no data can be presented on the data output lines. The state of RRCXX+ does not affect internal timing.

Internally Generated Timing

A memory cycle is initiated by the simultaneous assertion of the master clock input (MCSET+) and memory cycle enable (MEMCI+). If the memory is busy, input commands will not be accepted until the full memory cycle is completed. The memory is busy if either MBSYL- or RCYF1- is active.

Simultaneous assertion of MBSYL-, RCYF1-, MEMCI+ and MCSET+ will initiate a memory cycle. A flip-flop on the CM-003 μ-PAC will be set, generating a series of pulses. The timing of these pulses is determined by delay-line jumpers. The flip-flop is reset by

a signal from the delay line, thus controlling the output pulse width. Output pulse widths may be increased by performing an OR function at the inputs to the timing amplifiers on the CM-003. The reset output of the CM-003 flip-flop is used to generate a memory-busy indication during the first portion of a memory cycle.

Timing pulses generated by the CM-003 are used to (1) enable X- and Y- switches and sinks, (2) time the selection of X- and Y- switches and sinks, (3) generate a strobe pulse for the sense amplifiers, and (4) initiate a similar series of pulses at the write timing distributor. No strobe pulse is generated by the write timing distributor.

The strobe pulses (STRB1+X) sample the core signal during the read portion of the cycle. The sampling interval is chosen for appropriate signal and noise conditions.

The read CM-003 generates a read pulse on the ENSK1+ outputs, enabling the X- and Y- current sinks selected by the decoded address. The selected X- and Y- switches are then enabled by the ENYSW+ signal. The read-write interchange is implemented by gating the Y10XX input with RYSW+, RSKA1+, WYSWA+ and WSKA1+. YSWRL+ or YSWRH+ are never true simultaneously (if one is a read pulse, the other must be a write pulse). Both signals turn on Y- switch currents. Similarly, Y- sink activate pulses YSKRL+ and YSKRH+ are generated by interchanging RSKA1+ and WSKA1+ as a function of Y10XX.

Regeneration Loop

A block diagram of the regeneration loop for bit 1 is shown in Figure 2-33. If a read operation is to be performed, the M-register in the CPU is reset within 330 ns after the start of a cycle. During the write portion of every cycle, input data will be available from the M-register no later than 600 ns after the cycle is initiated. When a read operation is performed, the M-register is set if the sense amplifier output is activated (0 volt = ONE).

There is one sense amplifier for every 4,096 cores. A bit read out of the core stack will be sensed by one of the sense amplifiers. The amplifier outputs are ORed together so that an output from either amplifier will set the corresponding M-register stage. The M-register output is gated with the read data timing signal (RDATA-). When the register is a ONE, the write Y- switch is turned on and the addressed core is switched to a ONE state. If the core output is a ZERO, the register remains reset, write Y- drive current does not flow and the selected core remains in the ZERO state.

The CM-032 μ-PAC (see Appendix for complete description) is used for the sense amplifier and cable driver in an 8K memory. A 4K memory uses CM-033 μ-PACs, which are the same as the CM-032 except that only one sense amplifier per bit is used.

Memory Retention

The magnetic core array does not require power to provide its static memory capability. A pulse of power is required to switch cores from one state to the other. However, the pulse is not necessary to hold cores in their respective states. Because of the retentivity of the core magnetic material, the cores will remain in the state to which they have been switched. If power is removed, or lost, the magnetic core array will retain stored information indefinitely.

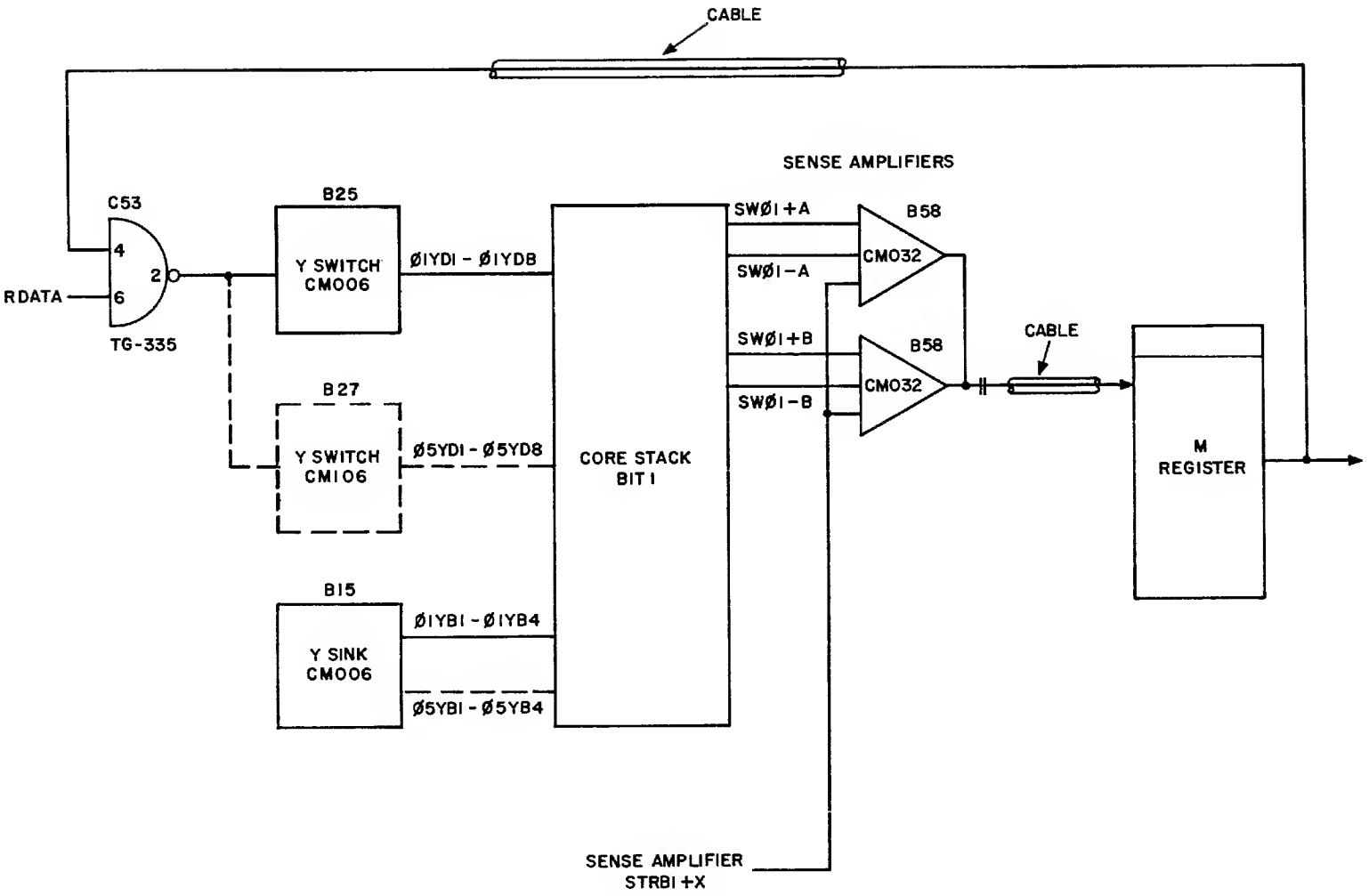


Figure 2-33. Regeneration Loop Simplified Diagram

POWER DISTRIBUTION

The memory dc power cable connects the memory to the RP-61 Power Supply. The dc power is distributed through the memory via laminated power buses, except for -6v which is wire wrapped to those PACs requiring this voltage. The dc and chassis grounds are isolated from each other. The memory coding drawing in Volume III shows memory dc power terminals. The 24v floating supply is referenced to ground by two resistors. The -24v and +24v outputs are approximately one-half the nameplate value when measured to ground (e.g., the +24v output is +11v to ground and -24v is -11v to ground when the 24v setting is 22v).

SECTION 3 - INPUT/OUTPUT TELETYPE INTERFACE

This section contains a discussion of the ASR-33/35 teletype interface logic. The interface logic is designed to function with either the ASR-33 or ASR-35. Either model of the ASRs and the interface logic provide the capability for reading paper tape, punching paper tape, generating hard copy from computer data, and providing a keyboard input to the computer. The teletype can be used in either on-line or off-line modes. The abbreviation ASR as used herein refers to either the ASR-33 or ASR-35.

The ASR is an input/output device that transmits data serially over a two-wire line. One line is the signal line and the other is the return line. When transferring a character from the ASR to the computer, the character is shifted serially over the signal line into a 9-bit buffer register. The transfer from the buffer register to the computer is in parallel (input mode). When a character is transferred from the computer to the ASR the process is reversed. The character is transferred in parallel via the output bus to the buffer register. The character is shifted through the buffer register and out over the signal line to the ASR (output mode).

An ASR character consists of an 11-bit code. It is made up of marks and spaces, analogous to logic ONE and ZERO. Approximately 65 ma of current in the signal line constitute a marking condition. No current flow indicates a space. The quiescent state of the ASR is the marking condition.

The first bit of an 11-bit character code is the start pulse and is always a space. Bits 2 through 9 are the information bits and can be any combination of marks and spaces. Bits 10 and 11 are always marks and denote the end of a character transmission.

NOTE

All referenced LBDs are contained in Volume III of this manual.

Figure 2-34 is a simplified block diagram of the interface logic as contained on LBDs 340, 341, and 342. The 2-phase clock is started and stopped as a function of a busy flip-flop in the sequence coatrol. The mode control logic sets the interface into an input or output mode as determined by the state of ADB10. The address decoder generates a teletype address signal whenever the address field of an I/O instruction is found to be XX04.

The sequence control is a group of flip-flops and associated gates which ensure the proper sequence of events within the interface. Note that the status of the buffer register influences operation within the sequence control, as well as the generation of shift pulses. The exact function and the buffer status is described in later text.

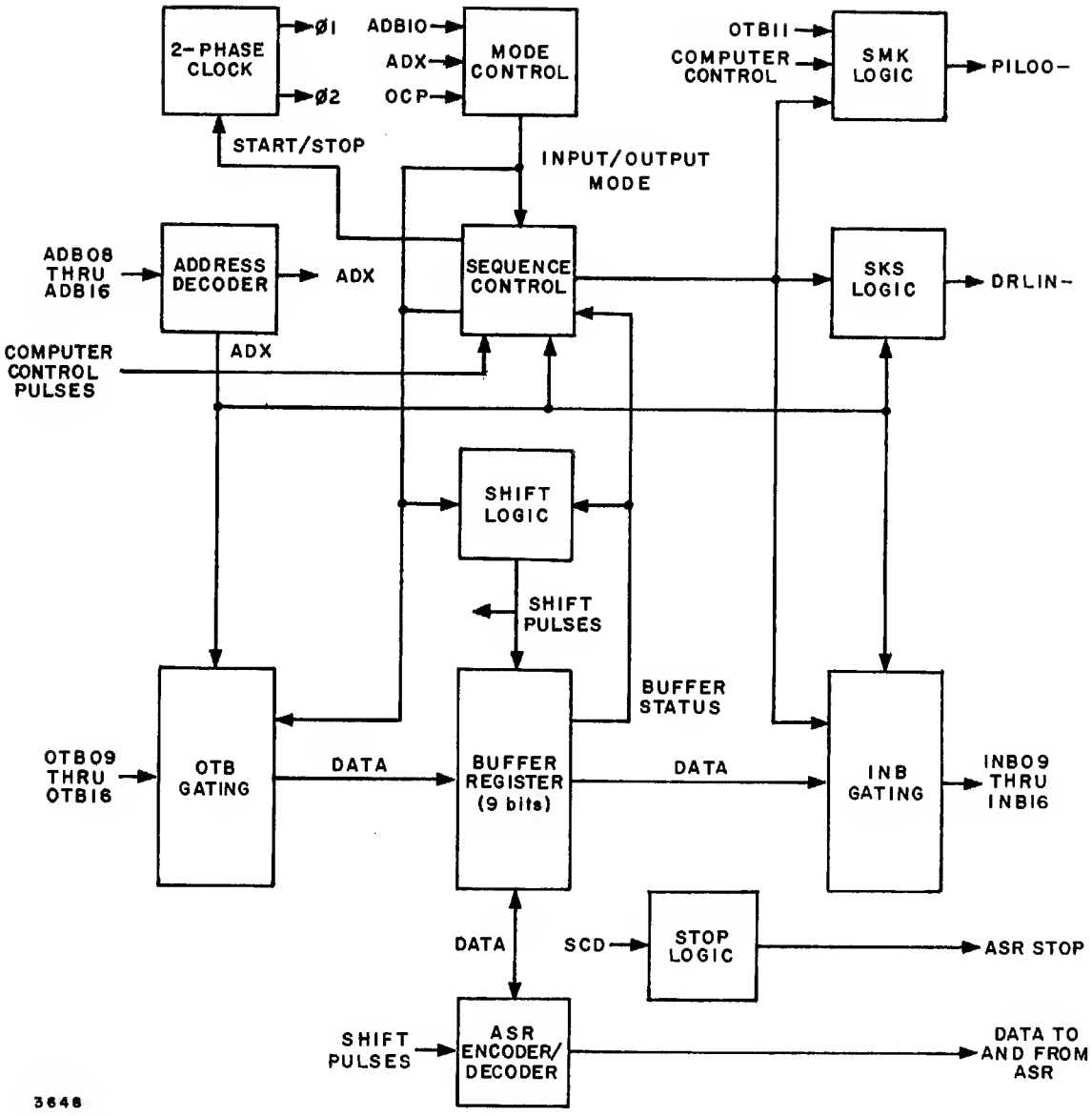


Figure 2-34. ASR Interface Block Diagram

The buffer register is a combination serial and parallel shift register. When transferring data in from the signal line, character information is transmitted via the ASR encoder/decoder. Transferring data out to the ASR is routed through the buffer register and ASR encoder/decoder.

The SKS logic generates the device ready signal in response to any of the ASR SKS instructions. (See Programmers Reference Manual, 3C Doc. No. 130071585.) The SMK logic generates a program interrupt request when the interface is ready and the SMK flip-flop is set.

The stop logic monitors the contents of the buffer register for an X-OFF character. When this character is present, a stop flip-flop is available for one character time for program test.

OPERATION

The following detailed discussion contains a description of interface operation in the input and output modes, each based on a timing diagram and LBDs 340, 341, and 342. The input mode discussion is given first.

Input Mode

Assume that an OCP '0004 (Enable ASR in Input Mode) is issued. As a result of this instruction, the interface logic receives an OCPLS- signal and a teletype address code (see LBD 342). The OCPLS- signal is used to generate signal OCPXX+. The address code generates signal TYADX-.

OCPLS- is used, in conjunction with TYADX+ and ADB10-, to generate signal TYICP- and to reset the output mode flip-flop TYOUT, LBD 342 E5. TYICP- generates PREST- which clears the buffer register and resets the TYRDY, TYK0X, TYK1X, and TYCFB flip-flops. This initializes the interface for input mode operation.

The next step is for the operator to strike a key on the ASR. This action causes TYDAT- to become passive (LBD 341 J10), and in turn causes TYDTA+ to become active. (See Figure 2-35 for Input Mode Timing Diagram.) This causes the busy flip-flop (TYBSY) to be set (LBD 340 L4). With TYBSY set, the clock is started (LBD 340 A1).

Note that all the conditions for the generation of the first of the two-phase clock pulses, TYK1P, are present at the input of gate L1A17C (LBD 340 E10). The trailing edge of TYK1P+ is used to set the TYCFA flip-flop in conjunction with signals TYSTP- and TYCAL+.

With reference to Figure 2-35, note that as the clock cycles, the TYK0X flip-flop is reset, enabling the generation of the second of the two-phase clock pulses, TYK2P (LBD 340 E11). With all inputs to gate L1C14C true, the first of nine shift pulses is generated (TYSFT). The function of this pulse is two-fold. First, it shifts data bits into the buffer register, and second, it keeps track of the number of data bits shifted into the buffer register.

The first shift pulse always stores a space in the LSB (least significant bit) of the buffer register. (When this space is propagated through the buffer register it is stored

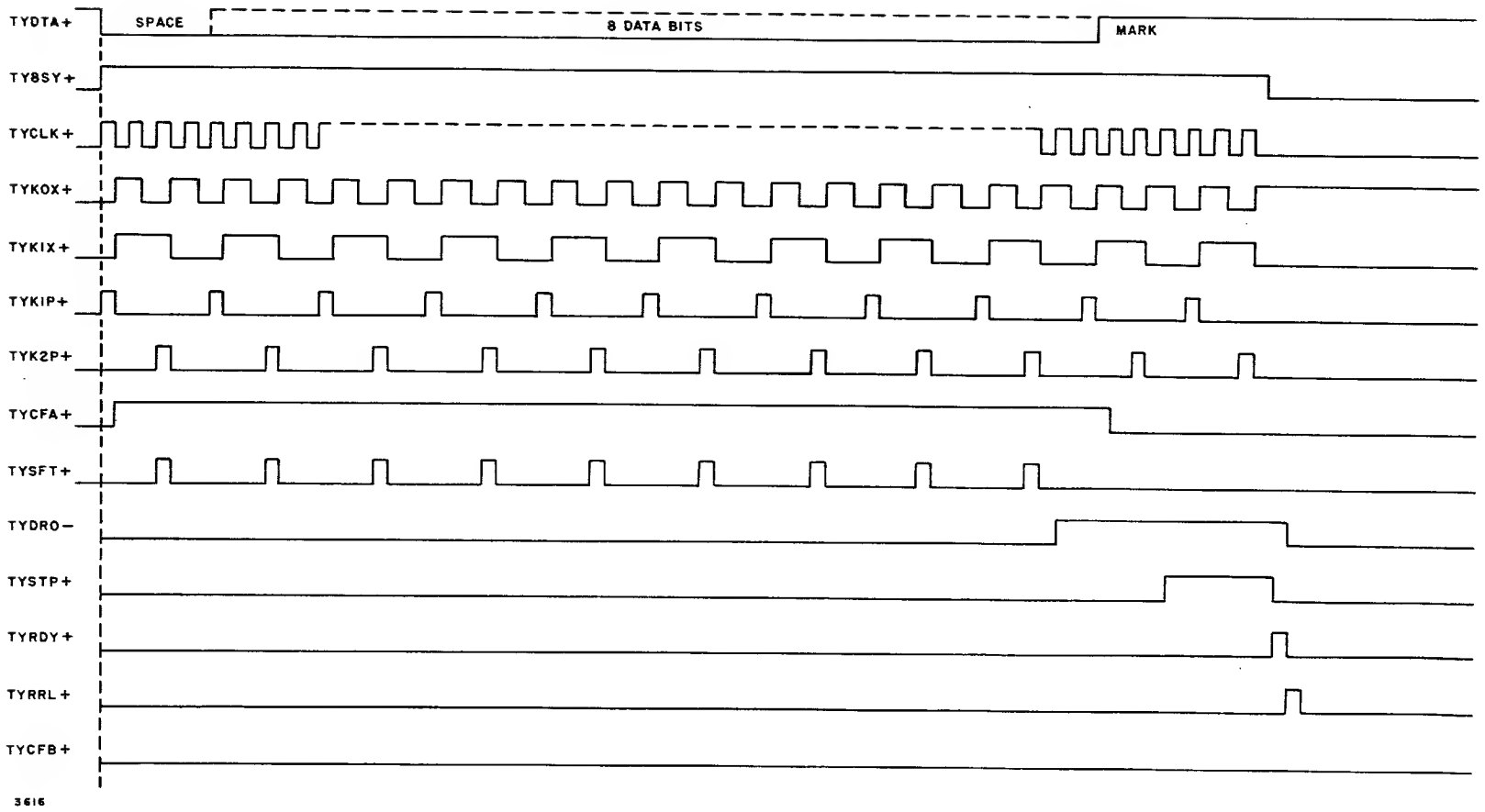


Figure 2-35. Input Mode Timing Diagram

in the TYDR0 flip-flop, a condition necessary to complete the loading and transfer of one teletype character.) After the generation of the first shift pulse, notice that the timing follows the pattern just described. The only thing that differs is that each new data bit generated (a total of eight for each character) is entered into TYDR0 and the previously entered data bits are propagated down the buffer register, with the lower order stages copying the next highest order stage.

After the ninth shift pulse, the space has been propagated through the buffer register and stored in TYDR0. The change in the state of TYDR0 resets the TYCFA flip-flop, in conjunction with TYOUT- and TYK1P+, inhibiting the generation of additional shift pulses. Further, with both TYCFA and TYCFB reset, the TYSTP flip-flop is set on the trailing edge of TYK2P+ (LBD 340 C5 and E5). Concurrent with the generation of the ninth shift pulse is the forcing of TYDTA to a mark condition. Since the TYSTP flip-flop is set, conditions are present at the input of the busy flip-flop to reset it at the trailing edge of TYSTP+, which stops the clock and sets the ready flip-flop TYRDY.

The CPU detects that the ASR has information to transfer in one of two ways: either by SKS '0004 or SKS '0204 (Skip if ASR is Ready in ASCII Mode, or Skip if ASR is Ready in Binary Mode); or by program interrupt on the PIL00- line if mask flip-flop TYMSK is set (LBD 342). As a result, either of four INA instructions is given INA '0004, '1004, '0204, or '1204) and the data is strobed into the CPU. The CPU signals the ASR that it will accept the data by generating signal RRLIN-.

RRLIN+ and TYADX+ generate signal TYRRL- which resets the ready flip-flop (LBD 342). TYADX- is used to strobe the contents of the buffer register onto the input bus (LBD 341). The interface is now ready for the next character from the ASR.

Output Mode

The output mode discussion is entered with the generation of an OTA. This is done to avoid complicating the discussion with events that occur prior to the generation of the OTA (during cycle).

Assume that an OTA '0004 is issued. A function of this instruction is to generate signal RRLIN-. RRLIN-, in conjunction with TYADX+ generates TYRRL- and in conjunction with TYADX+ and TYOUT+ generates TYOTP-. TYRRL- resets the ready flip-flop (TYRDY, LBD 342). (See Figure 2-36 for timing diagram.)

TYOTP- performs several functions. First, it resets TYDR0 in the buffer register (LBD 341). When TYDR0 is reset, the conditions for generating TYRCF- are no longer present to hold TYCFA reset. Then, it generates TYTCP- which sets the busy flip-flop (TYBSY, LBD 340). TYOTP+ is used to load the data from the output bus into the buffer register (LBD 342). The trailing edge of TYOTP+ sets the TYCBC flip-flop, making TYDTA+ true.

With both TYDR0 and TYCFB reset, conditions are present to set TYCFA with the first TYK1P+ (see TYCAL, LBD 340). Further, note that the inputs to signal driver/receiver L1A16 are both ZERO, causing a space to be sent to ASR (TYSIG- drops to less than 3 ma, the space condition).

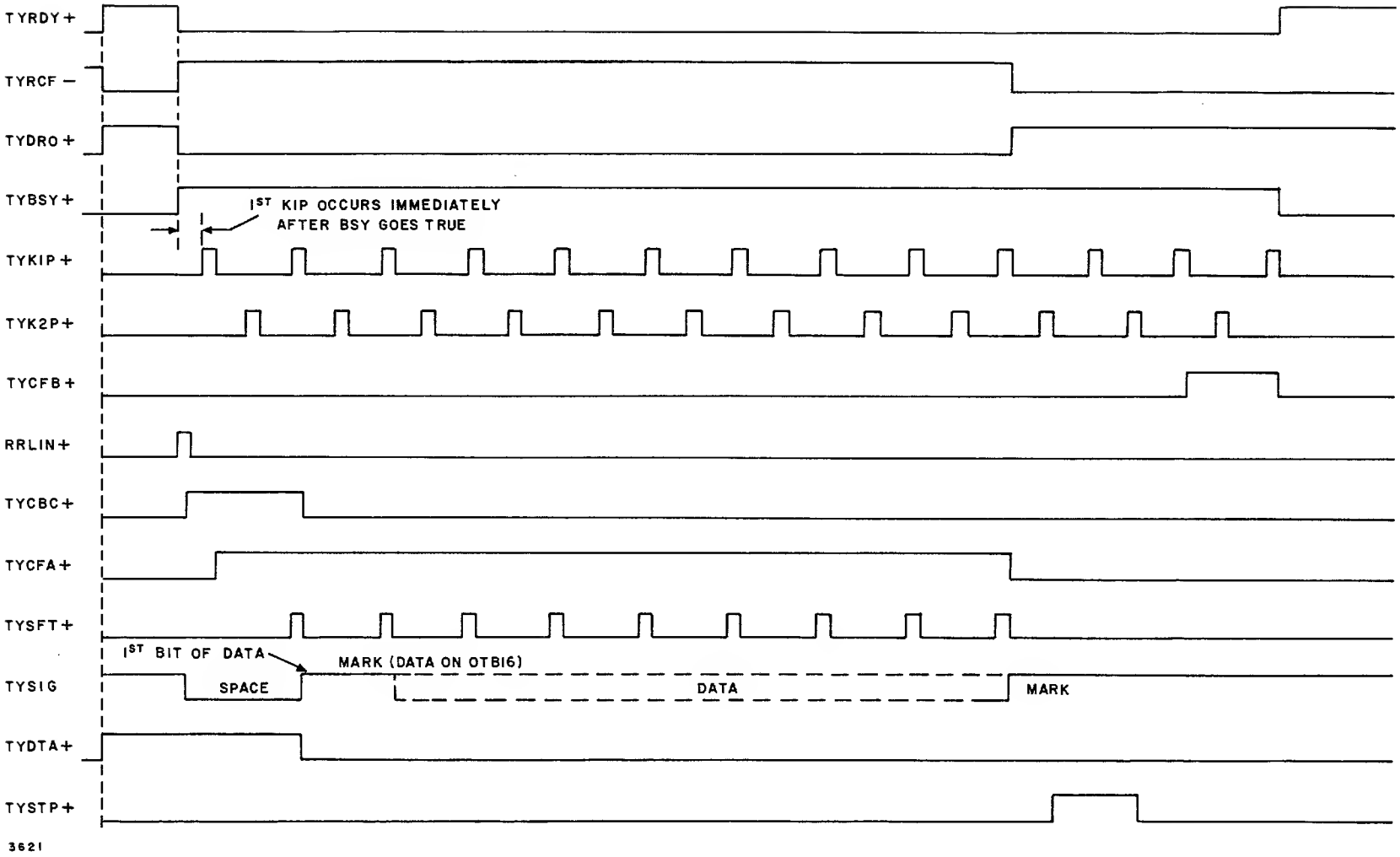


Figure 2-36. Output Mode Timing

A great deal has occurred in the previous paragraphs. Let us temporarily stop time and examine the events more closely to see the logic behind what has happened. First, the ready flip-flop (TYRDY) was reset to inform the CPU that the interface is involved in a data transfer. This condition is tested by an "if ready" SKS. Second, the busy flip-flop (TYBSY) is set. The condition is tested by an "if not busy" SKS. Now the CPU knows that the ASR is both "busy" and "not ready" and cannot accept or provide data until the present operation is terminated.

The busy flip-flop enabled the clock to run, permitting the sequence control logic to initialize prior to the acceptance of data from the output bus. When the character is transferred from the CPU to the interface, the OTB gating logic stores the character in the buffer register, enabled with internal control signal TYOTP+.

Now consider what remains to be done. The buffer register contains a character that needs to be transferred to the ASR. Since the ASR input must be serial, some means of serial entry must be provided. Further, it is important to keep track of the data bits in order to determine when the last bit has been routed to the ASR. This is implemented by shifting the data bits, one at a time, into the TYDR0 flip-flop. Since the signal driver/receiver is sensitive to the state of TYDR0, each bit shifted into TYDR0 is sent to the ASR as a mark or space. As the data bits are shifted through the buffer register, ZEROs are pushed into the buffer register, one at a time, as a function of the shift pulses and the reset state of the TYCBC flip-flop. Now let time start again to generate the first shift pulse.

In examining the inputs to gate L1A17B, note that the states of these inputs are such that signal TYSFT+ (shift pulse) is generated. TYSFT+ shifts the contents of the buffer register down one position and on its trailing edge, resets the TYCBC flip-flop. (See LBD 341.) This unconditionally puts a ONE in TYDR8 and sends the first data bit to the ASR via the signal driver/receiver (L1A16). Each successive shift pulse enters a ZERO into TYDR8 and shifts the data bits through the buffer register to the ASR.

With the generation of the ninth shift pulse note that the inputs to gates L1B13F, C, and D reflect the contents of the buffer register. This causes signal TYRCF- to be generated which in turn resets the TYCFA flip-flop, inhibiting the generation of additional shift pulses. As a result, a marking condition is presented to the ASR.

The operation is terminated when the TYSTP and TYCFB flip-flops are set. The mutual dependence of these two flip-flops causes them both to become reset after the combination of TYCFB and TYDR0 resets the busy flip-flop which in turn stops the clock.

Dummy Cycle

The dummy cycle is necessary to give the ASR enough time to respond to a change from input mode to output mode. Figure 2-37 is a timing diagram that illustrates what happens in the interface when an OTA is given immediately after an OCP and when an OTA is given after the dummy cycle. Observe that when the OCP is issued, the busy flip-flop is set and the clock is started. The OCP also causes TYDR0 to be set and the remainder of the buffer register is reset. This makes TYRCF- true, resetting the TYCFA flip-flop (LBD 340).

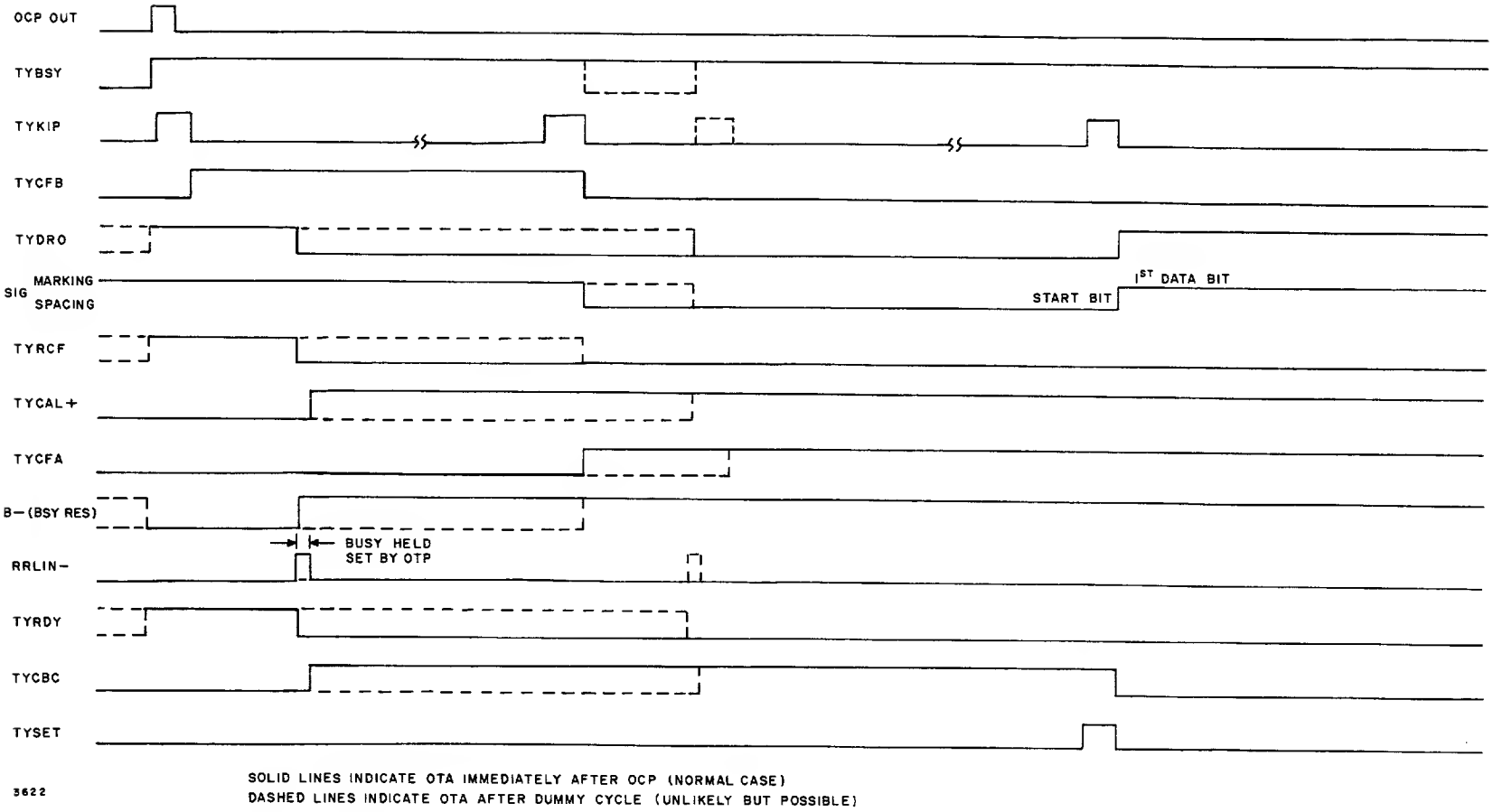


Figure 2-37. Dummy Cycle Timing Diagram

If the OTA is given immediately following the OCP, conditions are as described in the output mode discussion. However, if the OTA is given after the interface has generated a second TYK1P clock pulse, the busy flip-flop is reset, stopping the clock. (See dashed lines on Figure 2-37. In this second case, the clock is re-started by the OTA, the interface is re-initialized and ready to process the character from the CPU.

CHAPTER III
MAINTENANCE

This section contains general maintenance procedures for maintaining and troubleshooting the DDP-516 computer. Operating procedures are also included.

REQUIRED TOOLS AND TEST EQUIPMENT

Table 3-1 is the list of the tools and test equipment required for the maintenance of the computer. The items listed are not supplied with the computer.

Table 3-1.
Maintenance Equipment Required but Not Supplied

Qty	Description	Identification Number
1	Sweep delay oscilloscope*	Tektronix Model 585*
1	Dual-trace preamplifier*	Tektronix Type 82*
1	Multimeter	Simpson Model 270B
1	Solderless connection wrapping gun (μ-PAC)	917 200 001
1	Solderless connection wrapping tool (μ-PAC)	917 201 001
1	μ-PAC extraction tool	985 005 001
1	μ-PAC Extender PAC	XP-330
1	μ-PAC auxiliary solderless wrapping kit (includes wire stripper, burnisher, unwrap tool, and miscellaneous parts)	WK-330
1	Panel lamp assembly tool	Dialco W-500 1506-0500
1	Panel lamp extraction tool	Minneapolis-Honeywell 15PA32
1	Precision DC Voltmeter	Weston Model 931-1905003 30/7.5/3 volts, ±1/2% 1K ohm/volt

* A Tektronix Model 453 Oscilloscope may be used in place of the item listed.

μ-PAC LOCATIONS

The location of the μ-PACs in the CPU is shown in LBD 100 included in Volume III of this manual. Optional equipment locations are given in the respective option manual.

PAC HANDLING AND REPAIR PROCEDURES

Inserting and Removing System PACs

CAUTION

Turn off dc power before inserting or removing circuit cards. Failure to turn off the power might damage the PAC.

a. Insert μ-PAC modules by engaging the μ-PAC in the appropriate slot of the μ-BLOC and pressing the μ-PAC into position until the connector engages and sets. The μ-PAC module is inserted with components on the bottom.

b. Remove μ-PAC modules from μ-BLOCs by engaging the two holes at the handle end of the μ-PAC with the μ-PAC extractor tool. A 20-lb force is sufficient to disengage any μ-PAC from its mating connector. The μ-PAC can then be removed with the fingers.

PAC Troubleshooting

The Extender PAC, Model XP-330 permits access to points on the PACs. Signals on the pins of the PACs may be ascertained from the PAC descriptions. Leads for observing current waveforems using an ac current probe are provided on special extender PACs.

Component Checking

Many PACs have several identical channels. In most cases components can be checked by resistance comparison with parts on other channels or other PACs.

a. Transistor Checking. Transistors on a PAC can be checked with an ohmmeter. Do this carefully to avoid damaging the transistors by large meter currents. Check the base-emitter and collector-emitter junctions in both directions, using the meter scale which will apply the least amount of current to the transistor and still provide a reading. Replace any transistors having open or shorted junctions, or whose resistance readings differ considerably from those obtained on a transistor on an identical channel or PAC.

b. Diode Checking. Check diodes by comparing their forward and back resistances with diodes of the same type on other channels or PACs.

c. Resistors and Capacitors. Free one end of the resistor and check its resistance by using an ohmmeter in the conventional manner. To check most small capacitors for open circuits, a vacuum-tube ohmmeter is needed to induce a needle "kick."

Component Replacement

a. Use only top quality rosin-core 60/40 solder (60% tin, 40% lead).

b. Use a small hot soldering iron. Use a heat sink on the lead of the component, in the form of a pair of pliers or an alligator clip, to conduct heat away from the body of the component while soldering.

c. Remove excess solder from the etched side of the printed circuit board. Use a piece of large-diameter spaghetti or a commercially available tool for removing excess solder from eyelets.

d. Insert the leads of the new component into and through the drilled hole or eyelet, clip off excess wire, and solder from the etched circuit side of the PAC.

e. Examine the PAC carefully for excess solder. Remove resin deposits with a commercial cleaning solvent. Wipe the PAC clean with a dry lint-free cloth.

Maintenance Inspection

Conduct a visual inspection periodically. Watch specifically for accumulations of dust and dirt, improperly seated PACs, and damaged or improperly dressed cable and signal leads. Check that all connectors are securely mated, all air barriers are in place, and all cooling fans are operating.

COMPUTER SYSTEM PREVENTIVE MAINTENANCE

Clean the air filters on a 2 to 4 week basis, depending on the dust content of the surrounding air. If the dust content is severe, daily inspection is recommended. The filters can be cleaned by immersion in soap and water.

COMPUTER SYSTEM TROUBLESHOOTING

Computer system troubleshooting procedures include electrical and mechanical inspection, power supply troubleshooting, and logic PAC substitution.

Corrective Maintenance Inspection

Before beginning troubleshooting procedures, a thorough inspection of the system should be performed. Check that the system is not physically damaged and that no wires have been torn accidentally from the equipment. Make sure that electrical connectors and PACs fit firmly in their sockets.

Maintenance for the computer system consists largely of conducting prescribed diagnostic routines in conjunction with the controls on the Control Panel to localize equipment malfunctions. The indications provided on the Control Panel will help locate the trouble areas within the system.

PAC Substitution

Replacing suspected packages with those known to be operating properly is the quickest procedure for logic circuit troubleshooting. Troubleshooting at this level is best accomplished with a thorough understanding of principles of operation, and with the use of all other aids, such as the timing diagrams and flow charts in Volume II, the logic diagrams in Volume III, and the circuit descriptions in the μ-PAC instruction manuals.

Faulty packages can be repaired by referring to the appropriate PAC circuit description, schematic, and assembly drawing, and then isolating and replacing the faulty component(s) by using the list of replaceable parts.

Single Pulse Operation

The computer can be placed in the single pulse mode by the insertion of a jumper wire between A1D3530 and A1E3415. This jumper allows sense switch 4 to control the single pulse mode. With sense switch 4 up, each time the start button is pressed, a single timing level is executed. With sense switch 4 down the jumper has no effect.

In the single pulse mode, memory cannot be accessed. Any attempt to enter into registers will cause erroneous operation.

MEMORY MAINTENANCE PROCEDURES

General and detailed maintenance data and procedures are given in the following paragraphs to assist maintenance personnel in the troubleshooting and maintenance of the computer memory.

Visual Inspection

Conduct a visual inspection periodically. Watch for accumulation of dust, dirt, improperly seated PACs, and damaged or improperly dressed cable and signal leads. Check that all connectors are securely mated and that the cooling fans are operating properly. Clean fan filters periodically.

Preventive Maintenance Procedures

The memory is thoroughly tested prior to installation in the computer. All planes are tested simultaneously under all ZEROs, all ONEs, and worst-pattern conditions. The drive voltage and strobe timing are set so that optimum operating margins result. The memory should be tested periodically, as a preventive maintenance procedure, by using a memory test program.

Drive Voltage Calibration Procedure. -- The drive line currents are determined by the setting of the 24-vdc supply and the precision resistors which are mounted on the resistor plates. The 24v supply RP-61 is temperature compensated by a thermistor which is mounted near the core stack. The 24v supply calibration should be periodically checked according to the following procedure.

Turn on the ac power to the RP-61. Use a voltmeter capable of reading the voltage within ±1%. The optimum +24 volt supply setting shall be determined for each power supply connected to a memory, while running program X16-CMT1. All measurements shall be made at the memory. The minimum and maximum values shall be determined by decreasing and increasing the +24 volt supply and recording the last loaded value, minimum and maximum, at which the memory operates without error (do not exceed +32 volts). If the end of the adjustment range is reached prior to an error, consider the limit obtained as the minimum or maximum value. The optimum value (loaded value) shall be the average of the upper and lower limits. The final setting shall be greater than 1 volt from the upper and lower limits and within 2 volts of the stack nameplate value.

Logic Voltage Calibration

The +6-volt and -6-volt RP-61 supplies are not temperature compensated, so they can be calibrated in the conventional manner. The +6-volt and -6-volt logic supplies should be monitored at the memory using a voltmeter capable of reading the voltage within ± 1%. The +6-volt and -6-volt supplies should be set to their nominal values (+6.0v and -6.0v) while a program is being run in the memory. They can vary typically ±5% from their nominal values without causing memory errors.

Strobe Timing Calibration. -- The timing of the sense amplifier strobe pulse is set for each unit to give optimum operating margins. The core stack nameplate shows the time between the leading edge (1.5v point) of the RXSWA+ and STRB1- signals. It should not be necessary to adjust the strobe timing. If a change in timing is required to obtain proper memory operation, the associated PACs should be checked (e.g., CM-006, CM-032/CM-033, and PA-335) before a timing change is made. The CM-003 description in the appendix should be referred to if a timing change is required.

Corrective Maintenance Procedures

Corrective maintenance procedures consist of electrical and mechanical inspection and memory system troubleshooting.

Corrective Maintenance Inspection. -- Before beginning troubleshooting procedures, a thorough inspection of the system should be performed. Check that the system is not physically damaged and that no wired have been torn accidentally from the equipment. Make sure electrical connectors and PACs fit firmly in their sockets.

Memory System Troubleshooting Procedures

Memory system troubleshooting consists of determining the type of problem, predicting the μ-PAC at fault, and locating the faulty circuit. Test procedures to aid in troubleshooting are listed below.

CAUTION

Use oscilloscope probes carefully to avoid shorting of connector terminals resulting in damage to the PAC.

a. Sometimes, spare PACs may be used to isolate faulty circuits by interchanging identical PACs and noting any shift in the faulty bits or addresses. All memory PACs are interchangeable except the Timing Distributor PAC, Model CM-003, which has jumper wires for delay line timing.

b. Refer to PAC schematic and assembly drawings in the appendix to isolate the defective components on the printed circuit card. Replace defective components.

c. Memory failures are generally of the following types:

1. Operation failures, which are caused by faulty timing and control circuits.
2. Partial data word failures caused by a faulty sense amplifier, or data regeneration circuits.

3. Address failures caused by faulty selection circuits.

d. Memory failures may be localized by the following procedure:

1. Load the test pattern into the memory.

2. Initiate a read operation at each address sequentially and check each read-out data word for the following failures:

(a) Operation failures: No apparent response to commands applied to the memory, or faulty operation at all addresses (Table 3-2)

(b) Partial data word failures: Failures of one bit or series of two or more bits at all addresses (Table 3-2)

(c) Address failures: Faulty memory operation at particular addresses only (Table 3-2)

3. These procedures may sometimes be accelerated by the continuous memory access mode. The computer can be placed in the continuous memory access mode by the insertion of a jumper wire between A1B3304 and A1D3519. This jumper enables sense switch 1 to control the continuous memory access mode. With the machine in the memory access mode and sense switch 1 up, when the start button is pressed, memory will be accessed at a 1 mc rate.

Table 3-2.
Failure Modes and Probable Causes

	Symptoms	Probable Fault
Operational Failures	No apparent response to commands	1. D.C. Voltage 2. Loose or damaged cable PACs 3. CM-003 PAC failure 4. BANKX- passive 5. Timing and control fault: MCSET+, MEMCI+, MBSYL- and RDATA- signals
	Unable to read from any address	1. Read and Write CM-003 PACs interchanged 2. 24V supply 3. STRB1+ signal 4. RRCXX+ command 5. BANKX- signal
Partial Word Failures	Failure of one bit (ZERO or ONE) at all addresses	1. Sense Amplifier PAC 2. Y-Switch or Sink PAC 3. TG-335 circuit 4. Sense winding 5. Data input missing
	Failure of one bit at certain combinations of binary address digits	1. Sense Amplifier PAC 2. Y-Switch or Sink PAC 3. Y-Drive line 4. Y-Selection diode
	Failure of one bit at one address	1. Marginal voltages 2. Marginal Sense Amplifier PAC
	Failure of four bits at particular addresses	1. Y-Switch PAC 2. Backplane resistors

Table 3-2. (Cont)
Failure Modes and Probable Causes

	Symptoms	Probable Fault
Address, Decoding and Selection Failures	All bits fail as a function of particular address bits	1. X-Switch or Sink PAC 2. CM-003 PAC 3. X-drive line 4. PA-335 PAC 5. X-Selection Diode 6. Loose cable PAC or missing address input signal

Maintenance of Memory Magnetic Core Stack

CAUTION

Use extreme care when taking these measurements to avoid damaging the matrix windings.

Under normal operating conditions, it is unlikely that troubles will occur within the magnetic core stack. However, continuity measurements of the sense and drive windings will enable maintenance personnel to check core stack wiring.

Sense Windings. -- To check the memory sense windings perform the following:

a. Turn off memory power. Remove the Sense Amplifier PAC (CM-032 or CM-033) associated with the sense windings to be checked.

b. Place the ohmmeter leads across the sense winding inputs (SWXX+ and SWXX-) to the Sense Amplifier PAC as determined from the logic diagram. One sense winding links 4,096 cores. For 8,192-word memories, two sense windings must be checked for continuity.

c. Resistance readings should be approximately 10 ohms for all sense windings. The resistance readings for all bits should agree within ±10%.

Drive Windings. -- To check the memory drive windings, perform the following:

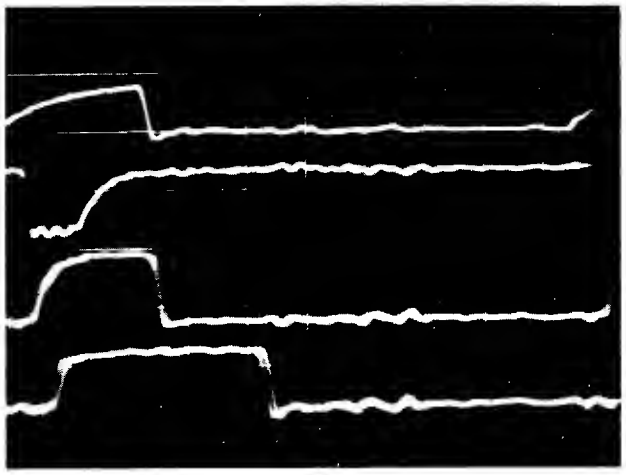
a. Turn off memory power. Remove the CM-006 and CM-106 Selection Switch PACs associated with the X- or Y-drive line to be checked. This can be determined from the logic diagrams and Tables 2-4, 2-5 and 2-6 by relating the bad address to a sink and switch output for both the X- and Y-coordinates. The drive winding connections to the core stack are shown in Figures 2-30 and 2-31 and the stack bit location (Figure 2-29).

b. Drive line resistance is a function of the core stack characteristics (number of bits, type and gauge of wire, and core spacing). The actual drive line connections are located on the printed circuit board of the core stack planes. The selection switch outputs are isolated by a diode from each drive line so that the resistance reading of any drive line will include a diode forward drop. The Y-drive line resistance is the same for all size memories

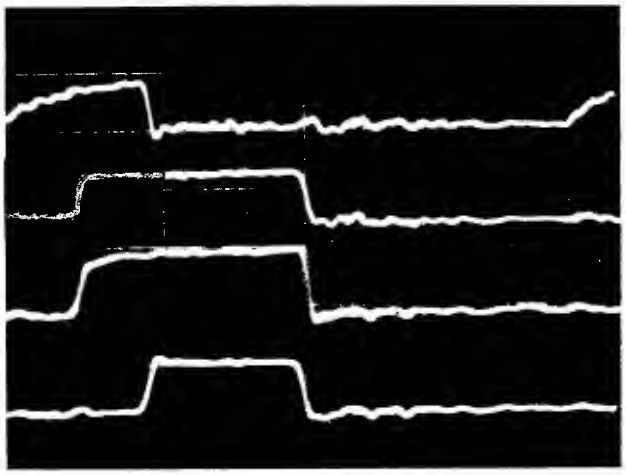
(nominally 1.6 ohms) while the X-drive line resistance is a function of word length only (nominally 2 ohms for a 16-bit memory).

c. Measure continuity by referring to the simplified selection diagram, Figure 2-32 and Chapter II decoding diagrams. For example, to check the continuity of drive line Y1, put one ohmmeter probe on the corresponding sink output (emitter output of transistor Q3) and the other ohmmeter probe on the proper switch output (collector of transistor Q2). A low resistance (one forward diode drop plus a drive line resistance given in the preceding paragraph) indicates continuity for both diodes and the drive line. It may be necessary to reverse the probes to obtain the correct polarity to forward-bias the selection diodes. The continuity of the current path for the opposite drive polarity should be similarly checked by moving the probe from the collector of Q2 to the collector of Q1 and reversing the polarity. A high resistance reading in both drive current polarity paths indicates an open drive winding or drive bus. If a drive bus is open, the other drive lines connected to the same bus will also have a high resistance reading. A high resistance reading in only one of the read or write current paths indicates an open F-08 Flat Pack diode. The Chapter II decoding drawings can be used to find the location of a defective F-08 or drive line.

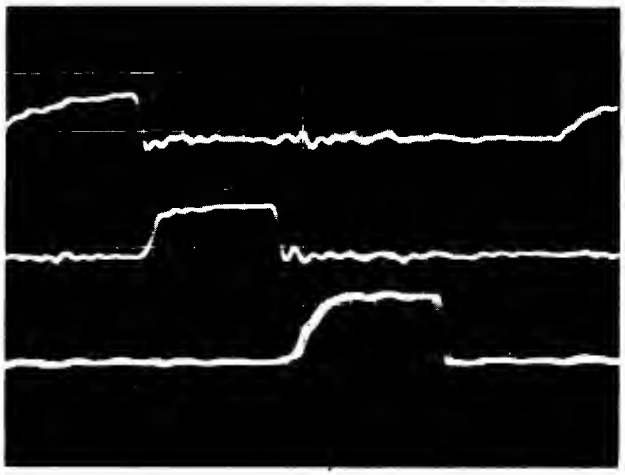
Waveforms are shown in Figure 3-1.



MEMCI+ C62-31
⚠ C61-04
RCYF+ C61-22
RENSK+ C61-30



MEMCI+ C62-31
RSKA1+ C61-25
RYSWA+ C61-5
RXSWA+ C61-29

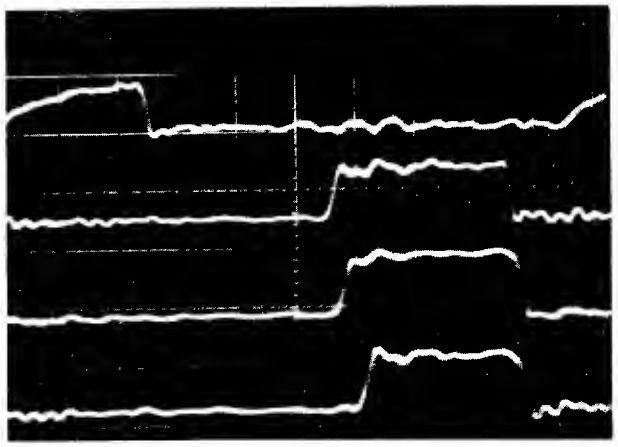


MEMCI+ C62-31
⚠ C61-26
WCYF1+ C51-22

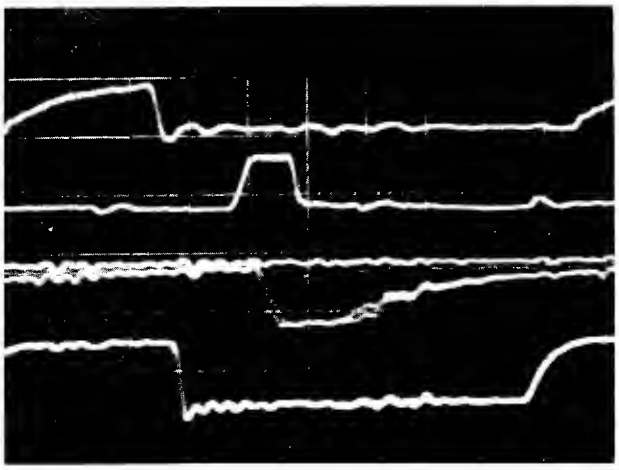
⚠ No signal name on LBD

5V/cm 0.1 μs/cm

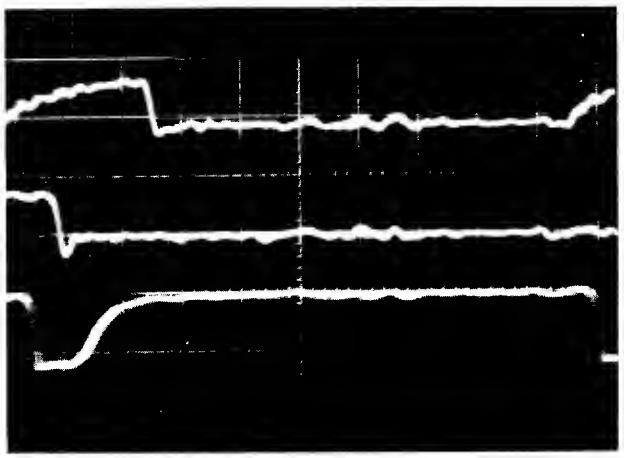
Figure 3-1. Waveforms (Part 1 of 6)



MEMCI+ C62-31
WENSK+ C51-30
WSKA1+ C51-26
WXSWA+ C51-16



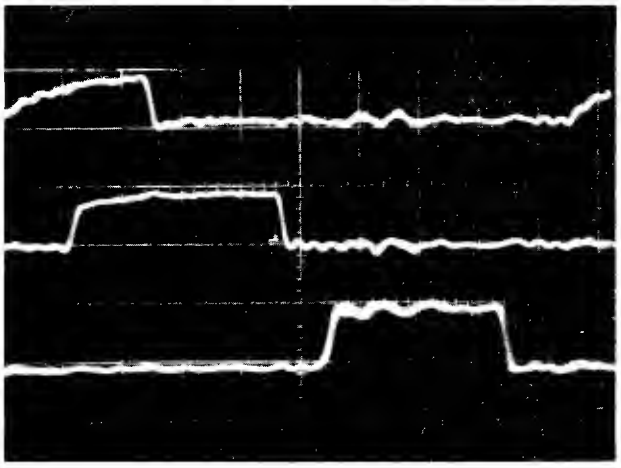
MEMCI+ C62-31
STRB1+B C63-15
MD01X- B58-5
MBSYL- C62-27



MEMCI+ C62-31
Y16XX+ A51-22
(1) C61-4

(1) No signal name on LBD
5V/cm 0.1 μs/cm

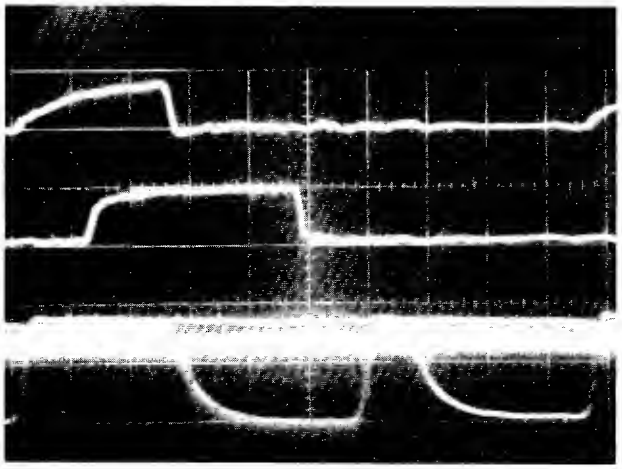
Figure 3-1. Waveforms (Part 2 of 6)



MEMCI+ C62-31

RENSK+ C61-30

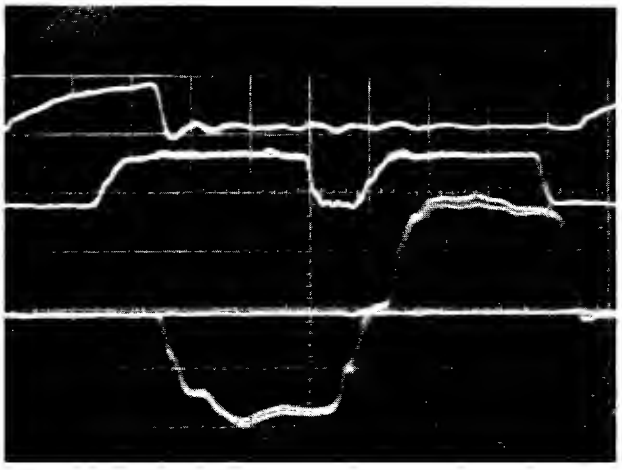
WENSK+ C51-30



MEMCI+ C62-31

RENSK+ C61-30

01YD1 B55-12
01YD2 B55-30 (1) (2)



MEMCI+ C62-31

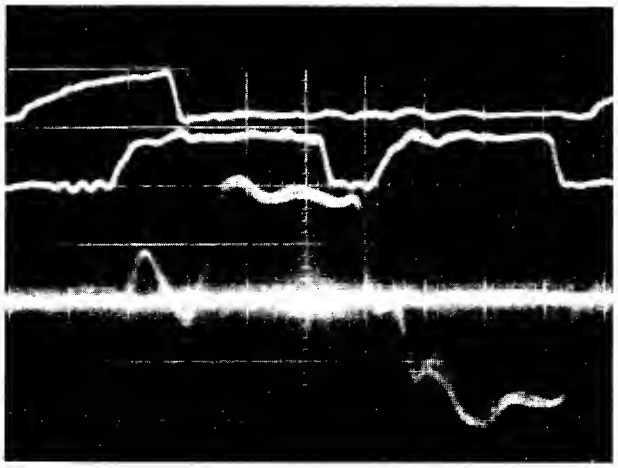
ENYSW+D C63-03

XD03 A51-06
XD04 A51-26 (1) (2)

(1) Currents at 200 mA/cm. All others are voltage waveforms at 5V/cm and 0.1 μs/cm

(2) Current probe reading both currents simultaneously.

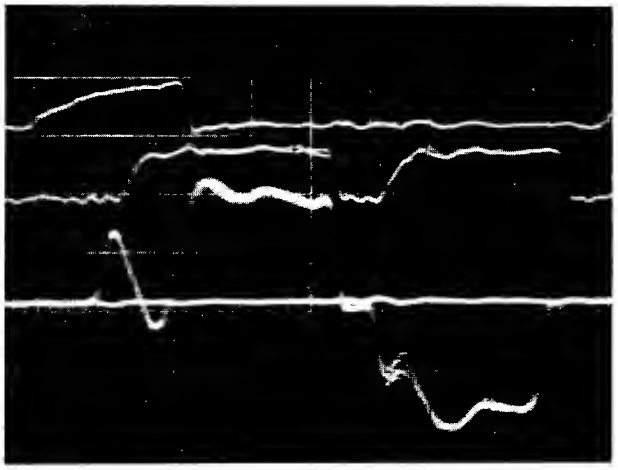
Figure 3-1. Waveforms (Part 3 of 6)



MEMCI+ C62-31

ENYSW+D C63-03

XB01 A63-12 A63-30 ⚠1



MEMCI+ C62-31

ENYSW+D C63-03

XB01 A63-12 A63-30 ⚠1 ⚠2

MEMCI+ C62-31

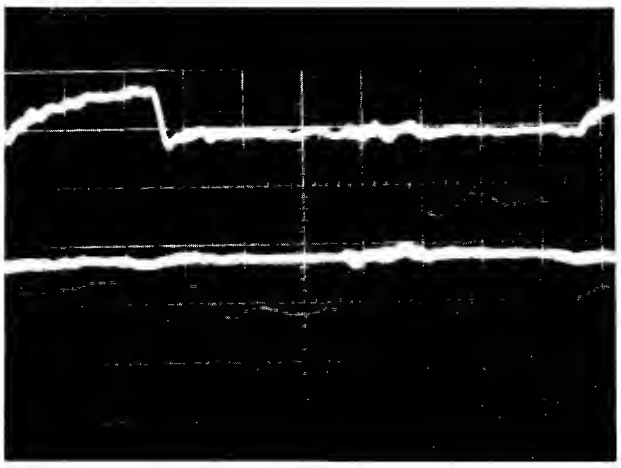
ENYSW+D C63-03

XB16 A57-04 A57-28 ⚠1

⚠1 Currents at 200 mA/cm. All others are voltage waveforms at 5V/cm and 0.1 μs/cm

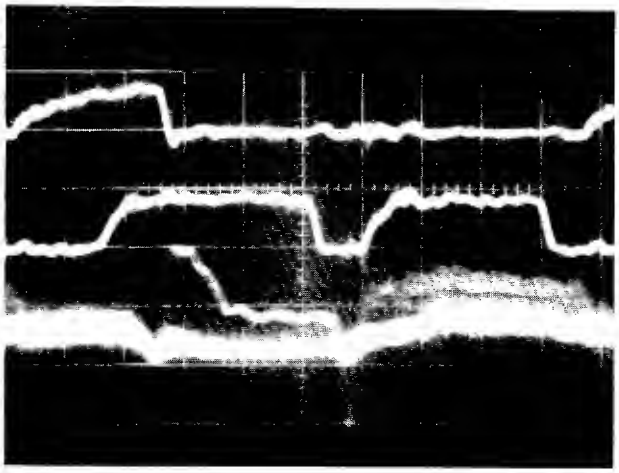
⚠2 Scope Sync for XBXX at Y09XX+A (B55-22)

Figure 3-1. Waveforms (Part 4 of 6)



MEMCI+ C62-31

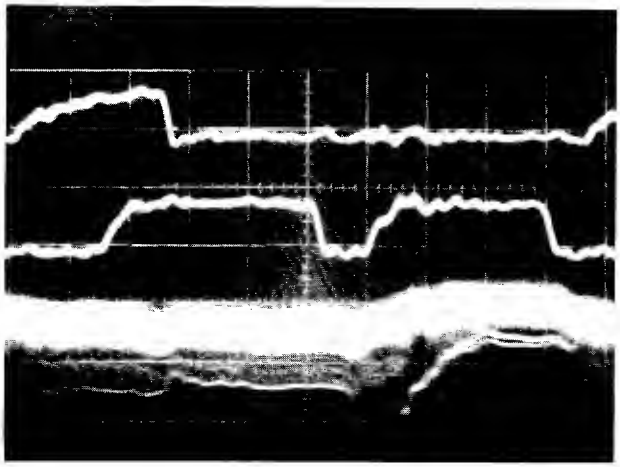
XB01 W1A01 ⚠1



MEMCI+ C62-31

ENYSW+D C63-03

XD01 A51-12 10V/cm



MEMCI+ C62-31

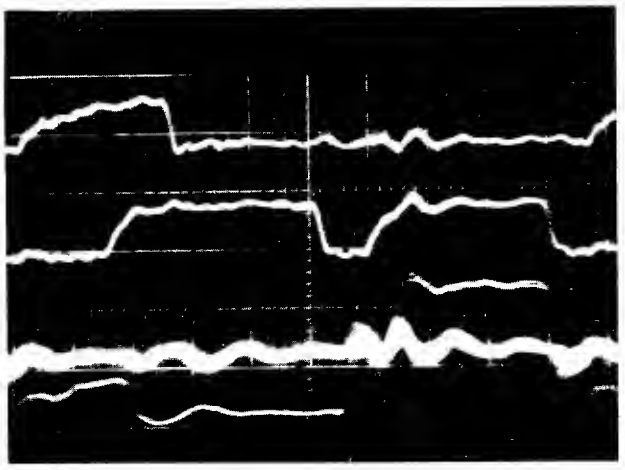
ENYSW+D C63-03

XD02 A51-30 10V/cm

All voltage waveforms at 5V/cm unless otherwise noted.

⚠1 Bottom X Board Terminal on Core Stack

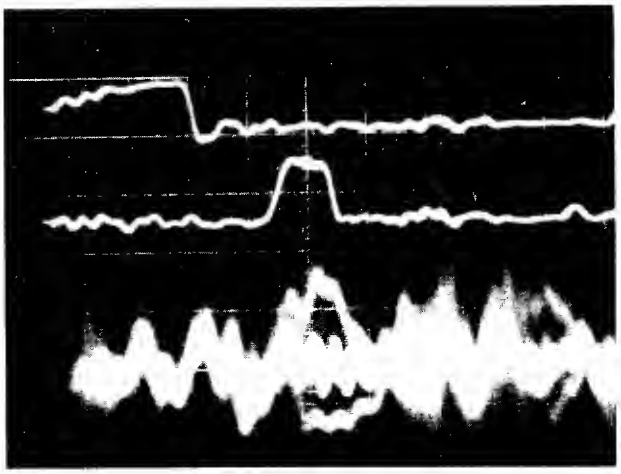
Figure 3-1. Waveforms (Part 5 of 6)



MEMCI+ C62-31

ENSK1+C C63-19

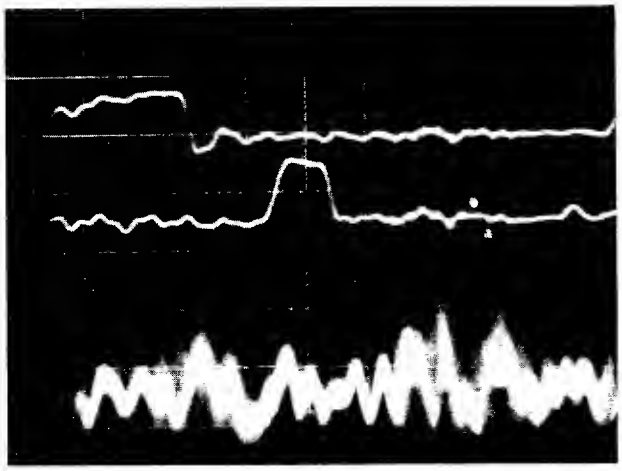
XB01 A63-12 A63-30 10V/cm



MEMCI+ C62-31

STRB1+B C63-15

SW05+A A68-01 ⚠ All
SW05-A A68-03 ONE's



MEMCI+ C62-31

STRB1+B C63-15

SW05+A A68-01 ⚠ All
SW05-A A68-03 ZERO's

⚠ Read with a differential scope preamp type 1A1 (50 mV/cm). All others are voltage waveforms at 5V/cm, and 0.1 μs/cm.

Figure 3-1. Waveforms (Part 6 of 6)

CHAPTER IV
PARTS LIST

This chapter contains the parts list for the DDP-516 General Purpose Digital Computer with 4K to 32K memory capacity. All electrical parts are listed and arranged in alphanumeric reference designation sequence. The reference designations are based on the DDP-516 coding drawings which are included in Volume III of this manual.

The description for each part listed includes the part name, brief technical data and the manufacturer's name and part number. The quantity required is for one next higher assembly regardless of assembly level. The 3C part number, when applicable, is given for each manufacturer's part number shown in the description. When there is no manufacturer's part number given in the description, 3C is the manufacturer and the part number is given in the 3C part number column.

Parts lists for all the μ-PAC digital modules are included with the μ-PAC data sheets found in the appendix of this manual.

Parts lists for the DDP-516 options are not included in this manual. They will be provided in associated documents.

Table 4-1.
DDP-516 Main Frame

Reference Designation	Description	3C Part No.	Qty Req
A1 Series	A1-UNIT -- CENTRAL PROCESSOR LOGIC	6013019-701	1
A1A23, 8, A1B24	μ-PAC DIGITAL MODULE -- universal flip-flop	Model CC-085	3
A1A24, A1D31, 4, A1E43, A1E52, 6	μ-PAC DIGITAL MODULE -- NAND gate Type II power amplifier	Model CC-073	6
A1A25, A1A41, A1C31, 8, A1C63, A1D27, A1D35, A1E56	μ-PAC DIGITAL MODULE -- transfer gate	Model TG-335	8
A1A26, A1A31, 5, A1A44, A1B28, A1B45, 8, A1B57, A1B61, 2, 7, 8, A1C43, 6, 7, A1C64, 8, A1E27, A1E31	μ-PAC DIGITAL MODULE -- NAND gate Type II	Model DL-335	19
A1A27, A1B27, A1B41, A1B63, A1C66,A1D32,6,7, A1E28, A1C45	μ-PAC DIGITAL MODULE -- NAND gate Type I	Model DI-335	12
A1A32, A1A43, A1B35, A1C55, A1E34, 7	μ-PAC DIGITAL MODULE -- expandable NAND gate	Model DN-335	6
A1A33, A1B32, 3, A1B55, 6, A1C41, A1C61, 2, A1E35	μ-PAC DIGITAL MODULE -- multi-input NAND gate	Model DC-335	9
A1B22, 3, A1B31, A1C22, 3, 4, A1C52,3,4,6,7,8	μ-PAC DIGITAL MODULE -- power inverter	Model PA-336	12
A1B53, A1D57	μ-PAC DIGITAL MODULE -- parallel transfer gate	Model CM-022	2
A1C27, 8	μ-PAC DIGITAL MODULE -- octal/decimal decoder	Model OD-335	2
A1C32, 3, 4, A1C51	μ-PAC DIGITAL MODULE -- NAND gate Type I power amplifier	Model CC-045	4
A1C37	μ-PAC DIGITAL MODULE -- master oscillator	Model CC-046	1
A1C42, A1E21, A1E52, 7, A1F52	μ-PAC DIGITAL MODULE -- pin jumper PAC (no components)	Model CC-054	5
A1D21 through 26	μ-PAC DIGITAL MODULE -- driver matrix	Model CC-002	6
A1D41, 3, 5, 7, A1D61, 3, 5, 7	μ-PAC DIGITAL MODULE -- columns PAY	Model CC-039	8
A1D42, 4, 6, 8, A1D62, 4, 6, 8	μ-PAC DIGITAL MODULE -- columns BEX	Model CC-037	8
A1E25	μ-PAC DIGITAL MODULE -- power failure sense	Model CC-043	1
A1E26	μ-PAC DIGITAL MODULE -- priority interrupt	Model CC-044	
A1E41 through 48 A1E61 through 68	μ-PAC DIGITAL MODULE -- column distribution register and memory information register	Model CC-038	16

Table 4-1. (Cont)
DDP-516 Main Frame

Reference Designation	Description	3C Part No.	Qty Req
A1E53	μ-PAC DIGITAL MODULE -- carry most significant	Model CC-034	1
A1E54	μ-PAC DIGITAL MODULE -- carry middle bits	Model CC-035	1
A1E55	μ-PAC DIGITAL MODULE -- carry least significant	Model CC-036	1
	MAIN FRAME DRAWER ASSY -- c/o PAC connector planes, cooling fans, swinging/locking mechanisms and associated parts; incl mtg provisions for two 1 x 3 connector planes for option use	6013019-702	1
A1A/B/C2 through 6, A1D/E/F2 through 6	.CONNECTOR PLANE ASSY -- c/o 5 x 3 module (15 connector blocks of 8 connectors each), framework and associated parts; factory repairable only	4013029-706	2
A1H	.FAN ASSY, AXIAL -- c/o 2 axial fans and associated parts; does not incl provisions for filter	4011031-705	1
A1H1A, 1C	..FAN, AXIAL -- 100 cfm; 105-120 vac, 50-60 cps; o/a dim. 1-1/2 in. h by 4-11/16 in. sq; ROTRON GOLD SEAL VENTURI MUFFIN FAN	964 001 002	2
A1H1B	..CONNECTOR, RECEPTACLE -- 3 hermaphrodite contacts; c/o the following individual items:		1
	... SHELL, CONNECTOR -- nylon; natural; accom 3 hermaphrodite contacts; snap mounts in panel cutout; ELCO 60-6501. 3218-00-000	941 333 001	1
	... CONTACT, ELECTRICAL -- fork type with one male and one female form one end and common solder term. with crimping tabs other end; accom No. 14-18 awg wire; ELCO 50-6501. 0312	941 402 001	3
	... RETAINER, CONNECTOR -- nylon; designed to assemble on each end of connector shell and hold mating connector by hooking action; ELCO 50-6501-3418	906 800 001	2
A1H2B	..TERMINAL BOARD -- barrier type; 5 terminals; CINCH-JONES 5-140	937 502 005	1
A1H3B	..FUSE, CARTRIDGE -- 0.5 amp, 125v; slo-blo type; 1/4 in. dia by 1-1/4 in. lg LITTLEFUSE 313.500 or BUSSMAN MDL1/2	960 001 014	1
A1H3B	..FUSEHOLDER -- accom 1/4 in. dia by 1-1/4 in. lg fuse; incl test prod hole; LITTLEFUSE 342012	935 002 001	1
A1H3B02/03 A1H3B04/05	..LINK, TERMINAL CONNECTING -- preformed jumper for barrier type term. board; brass, cad pl; CINCH-JONES 141-J	908 034 001	2
A1H3B03, 05	..CLIP, ELECTRICAL -- L-shaped; short leg fits quick-disconnect term.; long leg mounts on barrier type term. board contacts	1013913-001	2
A1K	.CONNECTOR ASSY -- c/o 15 connectors, 3 capacitors, and associated parts	3014214-701	1

Table 4-1. (Cont)
DDP-516 Main Frame

Reference Designation	Description	3C Part No.	Qty Req
A1K1A through 1Q	.. CONNECTOR, RECEPTACLE -- c/o the following individual items:		15
	... SHELL, CONNECTOR -- plastic; brown; accom single blade type contact; rect shape w/groove each side for snap mtg in panel; o/a dim. 1/4 in. w by 31/64 in. h by 31/64 in. lg; HEYMAN MFG DC202-1 BROWN	941 307 112	1
	... CONTACT, ELECTRICAL -- blade type; 0.032 in. thk; contact area 1/4 in. w; solder tab termination; press fit into shell; o/a dim. 21/64 in. w by 41/64 in. lg; HEYMAN MFG. T202-SS	937 201 004	1
A1K1A, 1B, 1D	... CAPACITOR, ELECTROLYTIC -- tantalum; 3.3 mf, 20%, 35 vdcw; rect epoxy case; radial leads; o/a dim. 0.170 in. thk by 0.225 in. h by 0.285 in. lg; KEMET K3R3P35	930 228 005	3
A1Z	. FAN ASSY, AXIAL -- c/o 2 axial fans and associated parts; incl provisions for mtg filter	4011031-701	1
A1Z1A, 1C	.. FAN, AXIAL -- same as ref. A1H1A	964 001 002	2
A1Z2B	.. TERMINAL BOARD -- same as ref. A1H2B	937 502 005	1
A1Z3B	.. FUSE, CARTRIDGE -- same as ref. A1H3B	960 001 014	1
A1Z3B	.. FUSEHOLDER-- same as ref. A1H3B	935 002 001	1
u/w A1Z	. FILTER, AIR -- multiple layers crimped wire screen cloth; aluminum frame; washable; o/a dim. 1/2 in. thk by 5 in. w by 13 in. lg; AIR-MAZE P56A, 5 x 13	911 003 004	1
	. LOCKING MECHANISM ASSY -- c/o guide rod, locking sleeve and associated parts	2011121-701	1
	. CABLE, WIRE -- 3/64 in. dia; cres; incl 1/16 in. dia cres hook attached one end w/swaging sleeve; o/a length 54 in.	1011538-701	1
	. PULLEY ASSY -- c/o circular groove pulley mtd in frame	2011304-701	2
	. HANDLE ASSY -- c/o cast bow handle w/integral mtg base and trigger to release locking mechanism	3011212-701	1
A21, 22, 23, 24, 25 Series	A2-UNIT -- POWER DISTRIBUTION	6013026-701	1
A21A1 through A8	CONNECTOR, RECEPTACLE -- 3 hermaphrodite contacts; c/o the following individual items:		8
	. SHELL, CONNECTOR -- nylon; blue; accom 3 hermaphrodite contacts; snap mounts in panel cutout; ELCO 60-6501.3218-00-172	941 333 004	1
	. CONTACT, ELECTRICAL -- same as u/w ref. A1H1B	941 402 001	3

Table 4-1. (Cont)
DDP-516 Main Frame

Reference Designation	Description	3C Part No.	Qty Req
	. RETAINER, CONNECTOR -- same as u/w ref. A1H1B	906 800 001	2
A21B1, B4, B7, A25E5	CONNECTOR, RECEPTACLE -- 2 female parallel blade contacts and 1 ground pin contact; rear panel mtd; screw term.; HUBBELL 5258	941 334 001	4
A22/A23	POWER SUPPLY -- provides indicator voltages; 3C 4013864-701	4013864-701	1
A22A1	. TRANSISTOR -- 2N3055	943 732 003	1
A22A1	. SOCKET, SEMICONDUCTOR DEVICE -- designed to mount T0-3 case transistor; MOTOROLA MK-10	935 251 001	
A22A2, A3	. CAPACITOR, ELECTROLYTIC -- 4000 mf, +100-10%, 40 vdcw; alum. case w/plastic sleeve; recessed screw term.; o/a dim. 2 in. dia by 3-1/8 in. lg; CORNELL-DUBILIER FAH-1475-1P	930 204 006	2
A22A2	. TRANSFORMER, POWER -- pri 115v, 60 cps; sec 25.2v center-tap, 2 amp; open frame; 5 wire leads 12 in lg; TRIAD F-41X	938 159 001	1
A22A3	. RECTIFIER, SEMICONDUCTOR DEVICE -- full-wave rectifier; input voltage 140v rms; output: 124 vdc res. load, 6 amps; case molded plastic; 4 solder lug term.; o/a dim. 0.625 in. h by 1.32 in. by 1.88 in. lg excl term.; MOTOROLA MDA952-3	943 409 001	1
A22B	. RESISTOR, VARIABLE -- composition; 10000 ohms 10%, 2w; linear taper; 1/4 in. dia slotted shaft 7/8 in. lg from mtg surface; 3/8-32 thd mtg bush 3/8 in. lg; 3 solder term.; MIL Type RV4NAYSD103A	933 005 014	1
A23	. ELECTRONIC COMPONENT ASSY -- c/o misc components mtd on 1/16 in. thk epoxy-glass board	2014040-701	1
A23A1	.. TRANSISTOR -- 2N3053	943 732 001	1
A23A4	.. RESISTOR, COMPOSITION -- 150 ohms, 5%, 1w; MIL Type RC32GF151J	932 005 029	1
A23B1	.. SEMICONDUCTOR, DIODE--1N971B	943 110 023	1
A23B4	.. RESISTOR, COMPOSITION -- 1000 ohms, 5%, 1/2w; MIL Type RC20GF102J	932 004 049	1
A23C1	.. RESISTOR, WIREWOUND -- 250 ohms, 10%, 10w; ceramic case; square shape; IRC PW 10-250-10%	932 207 020	1
A24A1	TERMINAL BOARD -- barrier type; 10 terminals with fork configuration and wire hole each end; CINCH-JONES 10-140W	937 502 110	1

Table 4-1. (Cont)
DDP-516 Main Frame

Reference Designation	Description	3C Part No.	Qty Req
A24A1	PLATE, DESIGNATION -- white numerals marked 1 through 10; black fiber; o/a dim. 1/32 in. thk by 1-1/8 in. w by 4-25/32 in. lg; CINCH-JONES MS10-140	982 003 009	1
A24B1	RELAY, ARMATURE -- two spst-NO (power) contacts rated 30 amp, 300 vac; two spst-NO (aux) contacts rated 3 amps, 300 vac; open construction; molded coil, 24 vac 50-60 cps, 8 ohms res; power term. 10-32 screws; aux term. 6-32 screws; o/a dim. 2-1/4 in. dp by 3-5/8 in. lg by 3-3/4 in. h; ARROW-HART & HEGEMAN MU-AA-20-00-XAX-24VAC-50/60CPS	963 017 001	
A24B2	TRANSFORMER, POWER -- same as A22A2	938 159 001	1
A24C1, A24D1	FAN, AXIAL -- same as ref. A1H1A	964 001 002	2
None	FILTER, AIR -- multiple layers crimped wire screen cloth; aluminum frame; washable; o/a dim. 1/2 in. thk by 4-1/4 in. w by 14-3/4 in. lg; AIR-MAZE P56A, 4-1/4 x 14-3/4	911 003 001	1
A24E1	RELAY, ARMATURE -- spdt; contacts gold alloy, rated 2 amp, 28 vdc non-inductive w/protective cover; coil 6 vdc, 510 ohms res, molded; solder term.; o/a dim. 1-7/16 in. dp by 1-9/16 in. lg by 1-1/2 in. h; RBM CONTROLS MS25-901	963 016 001	1
A24E2	TRANSFORMER, POWER -- pri 115v, 50-60 cps; sec 6.3v center-tap, 1.2 amp; open frame; 5 wire leads 6 in. lg; TRIAD F-14X	938 165 001	1
A25A1	CONNECTOR, RECEPTACLE -- red; c/o the following individual items:		1
	. SHELL, CONNECTOR -- plastic; red; accom single blade type contact; rect shape w/groove each side for snap mtg in panel; o/a dim. 1/4 in. w by 31/64 in. lg by 31/64 in. h; HEYMAN MFG DC202-1RED	941 307 212	1
	. CONTACT, ELECTRICAL -- blade type; 0.032 in. thk; contact area 1/4 in. w; solder tab termination; press fit into shell; o/a dim. 21/64 in. w by 51/64 in. lg; HEYMAN MFG T202-S	937 201 001	1
A25A3	METER, TIME TOTALIZING -- time range 0 to 9999.9 hours; 110-125 vac, 60 cps; 3-1/2 in. dia mtg flange; plastic case; 10-32 thd stud term; JBT INSTRUMENTS 31-EX	936 001 001	1
A25B1	CONNECTOR, RECEPTACLE -- black; c/o the following individual items:		1
	. SHELL, CONNECTOR -- same as A25A1 except color black; HEYMAN MFG DC202-1 BLACK	941 307 012	1
	. CONTACT, ELECTRICAL -- same as A25A1	937 201 001	1

Table 4-1. (Cont)
DDP-516 Main Frame

Reference Designation	Description	3C Part No.	Qty Req
A25C1	CONNECTOR, RECEPTACLE -- 7 female contacts; plastic body with 1/2-20 thd mtg bush; incl twist-lock ring to hold mating connector; AMPHENOL 126-198	941 318 001	1
A25D1	CONNECTOR, RECEPTACLE -- 9 female contacts; plastic body with 1/2-20 thd mtg bush; incl twist-lock ring to hold mating connector; AMPHENOL 126-221	941 318 003	1
A25E3, A25F3	CONNECTOR, RECEPTACLE -- brown; 2 contacts; c/o the following individual items:		2
	. SHELL, CONNECTOR -- plastic; brown; two sections, each accom blade type contact; rect shape w/groove each side for snap mtg in panel; o/a dim. 1/2 in. w by 31/64 in. lg by 31/64 in. h; HEYMAN MFG DC202-2 BROWN	941 307 122	2
	. CONTACT, ELECTRICAL -- same as A25A1	937 201 001	4
A25F1	CIRCUIT BREAKER -- 20 amp, 250 vac, 60 cps; single pole series trip; time curve 4; fungus and moisture resistant; 10-32 thd stud term.; HEINEMAN AM12MG6-20-250-60-4	960 054 006	
A25G2	FUSE, CARTRIDGE -- 0.5 amp, 250 v; 1/4 in. dia by 1-1/4 in. lg; instantaneous; LITTLEFUSE 312.500 or BUSSMAN AGC 1/2	960 002 005	1
A25G4	FUSE, CARTRIDGE -- 0.125 amp, 250v; 1/4 in. dia by 1-1/4 in. lg; instantaneous; LITTLEFUSE 312.125 or BUSSMAN AGC 1/8	960 002 002	1
A25H1	FUSE, CARTRIDGE -- 1 amp, 125v; slo-blo type; 1/4 in. dia by 1-1/4 in. lg; LITTLEFUSE 313.001 or BUSSMAN MDL 1	960 001 019	1
A25H2	FUSE, CARTRIDGE -- 1 amp, 250v; 1/4 in. by 1-1/4 in. dia by 1-1/4 in. lg; instantaneous; LITTLE-FUSE 312.001 or BUSSMAN AGC 1	960 002 007	1
A25H4	FUSE, CARTRIDGE -- same as ref A1H3B	960 001 014	1
A25H5	FUSE, CARTRIDGE -- 10 amp, 125v; 1/4 in. dia by 1-1/4 in. lg; instantaneous; BUSSMAN GLH 10	960 002 015	1
A25G2, G4 A25H1, 2, 4, 5	FUSEHOLDER -- accom 1/4 in. dia by 1-1/4 in. lg fuse; BUSSMAN HKP	935 003 001	6
A3 Series	A3-UNIT -- POWER SUPPLY, RP-61	4013982-701	1

Table 4-1. (Cont)
DDP-516 Main Frame

Reference Designation	Description	3C Part No.	Qty Req
	NOTE This power supply is procured from two sources: North Electric Co. and AULT, Inc. They are physically and electrically interchangeable. However, their component parts and quantities are not identical. Refer to Table 6-2 for the breakdown of the unit supplied by North Electric and to Table 6-3 for the breakdown of the unit supplied by AULT, Inc. MEMORY UNIT(S) For component parts of 4K through 32K memory configurations, refer to the applicable table as tabulated below: Table 6-4. 4K and 8K Memory Table 6-5. 12K and 16K Memory Table 6-6. 24K and 32K Memory Z-UNIT -- CONTROL PANEL		
Z1X1A, 1B, 1D through 1L, 1N through 1U, Z1X2H, 2U, 2V	SWITCH, PUSH -- momentary spdt; incl provisions for mtg T-1-3/4 min flange base lamp and lens (lamp and lens not incl); 6 solder lug term. designed for insertion into printed wiring board	934 265 001	20
Z1X1A,1B, 1D through 1L, 1N through 1U Z1X2H	LENS -- unmarked; black plastic body with flat white transluscent face, alum mtg bush; body 0.500 in. dia by 0.438 in. lg; DIALCO 186-37-5	908 276 071	18
Z1X2U	LENS -- same as Z1X1A except face color red; DIALCO 186-37-1	908 276 171	1
Z1X2V	LENS -- same as Z1A1A except face color green; DIALCO 186-37-2	908 276 271	1
Z1X1B, 1D through 1L, 1N through 1U, Z1X2V	LAMP, INCANDESCENT -- 28v; T-1-3/4 bulb, min flange base; GE 387	945 002 002	25
	NOTE Lamps not used at ref Z1X1A, Z1X2H, and Z1X2V		
Z1X2A	SWITCH, PUSH -- indicating type; green lens; alternating action (push ON, push OFF); c/o the following individual items:		1

Table 4-1. (Cont)
DDP-516 Main Frame

Reference Designation	Description	3C Part No.	Qty Req
	. SWITCH, PUSH -- spdt; alternate action; 5 amp, 250 vac; prime actuator not incl; designed to snap mount on lampholder; MICROSWITCH 2D100	934 263 001	1
	. LAMPHOLDER -- accom two min flange base lamps; also designed to mount and operate a push switch when assd with lens; single hole mtd w/4 integral retaining clips; MICROSWITCH 2M1	935 026 001	1
	. LENS -- insert marked HALT; black characters, 1/8 in. h; also functions as pushbutton for operating lampholder plunger and switch; mounts in lampholder	908 277 003	1
	.. LENS -- plastic; 3 pieces: green cap and base, transparent inserts; 1.030 in. dia; MICROSWITCH 2J8		1
	. RING, GUARD -- white; plastic; attaches to lampholder; MICROSWITCH 2K2	908 125 003	1
Z1X2A	LAMP, INCANDESCENT -- same as Z1X1B	945 002 002	Ref
Z1X2C	SWITCH, LEVER -- 3 position; center normal; position 1: 1 form D; position 2: 2 form A, 1 form B; locking, welded cross bar palladium contacts; 3 amp 200w max ac non-inductive load; rect black plastic knob: 15/32-32 thd mtg bush	934 020 003	1
Z1X2E,2F,2Q through 27	SWITCH, LEVER -- 2 position; center normal; position 1: 1 form C; locking; silver contacts; 3 amp, 300w, max, ac non-inductive load; rect black plastic knob; 15/32-32 thd mtg bush; SWITCHCRAFT 28203L	934 051 102	6
Z1X2G	SWITCH, LEVER -- 2 position; center normal; position 1: 1 form A; locking; silver contacts; 3 amp, 300w max, ac non-inductive load; rect black plastic knob; 15/32-32 thd mtg bush; SWITCHCRAFT 28201L	934 051 101	1
Z1X2J through 2P	SWITCH, PUSH -- indicating type; 6 pushbuttons w/white unmarked lenses; c/o the following individual items:		1
	. SWITCH, PUSH -- 6 stations; each station has 1 form A, 3 form C contact sets and provisions in plunger for mtg T-1-3/4 lamp; interlocked w/ lockout bar; contacts rated 3amp, 300w max, ac non-inductive load; lamp lights at IN position	934 260 002	1
	. PUSHBUTTON -- plastic; black; press fits on switch plunger; has provisions for mtg but does not incl lens; SWITCHCRAFT 405-02	908 280 002	6
	. LENS -- unmarked; white translucent plastic; rect shape w/contoured face; SWITCHCRAFT 401-05	908 279 007	6

Table 4-1. (Cont)
DDP-516 Main Frame

Reference Designation	Description	3C Part No.	Qty Req
Z1X2J through 2P	LAMP, INCANDESCENT -- 28v; T-1-3/4 bulb min flange base; GE 387	945 002 002	Ref
Z2XA1	CONNECTOR, RECEPTACLE -- 9 male contacts; plastic body with 1/2-20 thd mtg bush; incl twist-lock ring to hold mating connector; AMPHENOL 126-219	941 332 002	1
Z2XA3	FUSE, CARTRIDGE -- 1 amp, 250v; 1/4 in. dia by 1-1/4 in. lg; instantaneous; LITTLEFUSE 312001 or BUSSMAN AGC1	960 002 007	1
Z2XA3	FUSEHOLDER -- accom 1/4 in. dia by 1-1/4 in lg fuse; BUSSMAN HKP	935 003 001	1
Z2XB1	CONNECTOR, RECEPTACLE -- yellow; c/o the following individual items:		1
	.SHELL, CONNECTOR -- plastic; yellow; accom single blade type contact; rect shape w/groove each side for snap mtg in panel; o/a dim. 1/4 in. w by 31/64 in. lg by 31/64 in. h; HEYMAN MFG DC202-1 YELLOW	941 307 412	1
	.CONTACT, ELECTRICAL -- blade type; 0.032 in. thk; contact area 1/4 in. w; solder tab termination; press fit into shell; o/a dim. 21/64 in. w by 51/64 in. lg; HEYMAN MFG T202-S	937 201 001	1
Z2XB3	CONNECTOR, RECEPTACLE -- red; c/o the following individual items:		1
	.SHELL,CONNECTOR -- same as Z2XB1 except color red; HEYMAN MFG DC202-1 Red	941 307 212	1
	.CONTACT, ELECTRICAL -- same as Z2XB1	937 201 001	1
Z2XC1	CONNECTOR, RECEPTACLE -- green; c/o the following individual items:		1
	.SHELL, CONNECTOR -- same as Z2XB1 except color green; HEYMAN MFG DC202-1 GREEN	941 307 512	1
	.CONTACT, ELECTRICAL -- same as Z2XB1	937 201 001	1
Z2XC2	RELAY, ARMATURE -- dpdt; 1 sec delay; snap-action enclosed contacts rated 5 amp, 125/250 vac; coil 24vdc, 2w, continuous duty; moveable core w/ liquid damping; terminals push-on blade type; HEINEMAN BN1-522-XBX-24vdc	963 015 001	1
Z2XC3	CONNECTOR, RECEPTACLE -- white; c/o the following individual items:		1
	.SHELL, CONNECTOR -- same as Z2XB1 except color white; HEYMAN MFG DC202-1 WHITE	941 307 912	1
Z2XD1	CONNECTOR, RECEPTACLE -- black; c/o the following individual items:		1
	.SHELL, CONNECTOR -- same as Z2XB1 except color black; HEYMAN MFG DC202-1 BLACK	941 307 012	1

Table 4-1. (Cont)
DDP-516 Main Frame

Reference Designation	Description	3C Part No.	Qty Req
	. CONTACT, ELECTRICAL -- same as Z2XB1	937 201 001	1
Z3XA1, A2	CONNECTOR, RECEPTACLE -- 34 female contacts; each double leaf type w/each leaf terminated in taper pin socket (64 total); accom 3/64 in. thk etched board; METHODE ELECTRONICS RD-834-DTP	941 010 001	2
	CABLE ASSEMBLIES		
C1 (A25D1 to Z2XA1)	CABLE ASSY, SPECIAL PURPOSE -- 9 cond, no. 20 awg, cabled and covered w/insulating sleeve; one end 9-pin male connector; other end 9-pin female connector; o/a length 17 ft	1014550-701	1
A25D1	. CONNECTOR, PLUG -- 9 male contacts; incl twist-lock clips and hood w/cable clamp AMPHENOL 126-220	941 120 003	1
Z2XA1	. CONNECTOR, PLUG -- 9 female contacts; incl twist-lock clips and hood w/cable clamp AMPHENOL 126-222	941 136 001	1
C2 (A25C1 to A1K1F,G,H,J	CABLE ASSY, SPECIAL PURPOSE -- 4 cond, no. 20 awg, cabled and covered w/insulating sleeve; one end 7-pin male connector; other end of each conductor female quick-disconnect term.; o/a length 5 ft	1014555-701	1
A25C1	. CONNECTOR, PLUG -- 7 male contacts; incl twist-lock clips and hood w/cable clamp AMPHENOL 126-195	941-120-001	1
A1K1F,G,H,J	. TERMINAL, QUICK DISCONNECT -- female; accom 1/4 in. w by 0.032 in. thk blade male contact; crimp type ferrule for no. 18 - 22 awg wire; THOMAS and BETTS A250	937 200 002	4
C3 (A25A1 to A1K1K)	LEAD, ELECTRICAL -- no. 14 awg cond, brown; both ends female quick-disconnect term.; o/a length 30 in.	1014552-702	1
A25A1	. TERMINAL, QUICK DISCONNECT -- female; accom 1/4 in. w by 0.032 in. thk blade male contact; crimp type ferrule for no. 14-18 awg wire; THOMAS and BETTS RB250	937 200 001	1
A1K1K	. TERMINAL, QUICK DISCONNECT -- female; accom. 1/4 in. w by 0.032 in. thk blade male contact; crimp type ferrule for no. 14 - 16 awg wire; THOMAS and BETTS B250	937 200 003	1
C4 (A3 to A1K)	CABLE ASSY, POWER -- 5 cond, no. 14 awg, cabled and covered w/insulating sleeve; both ends each conductor terminated w/female quick-disconnect term.; o/a length 40 in.	1014556-701	1

Table 4-1. (Cont)
DDP-516 Main Frame

Reference Designation	Description	3C Part No.	Qty Req
A3A2C, A3A3C,E, F, A3A4E	. TERMINAL, QUICK DISCONNECT -- same as A25A1 u/w C3	937 200 001	5
A1K1A through 1E	. TERMINAL, QUICK DISCONNECT -- same as A4K1K u/w C3	937 200 003	5
C5 (A3 to Z3)	CABLE ASSY, POWER -- 5 cond. no. 14 awg, cabled and covered w/insulating sleeve; both ends each conductor terminated w/female quick-disconnect term.; o/a length 15 ft	1014554-701	1
A3A2D, A3A3A,B A3A4F, A3A5E, Z2XB1,B3, Z2XC1,C3 Z2XD1	. TERMINAL, QUICK DISCONNECT -- same as A25A1 u/w C3	937 200 001	10
C6 (A25B1 to A3A3D)	LEAD, ELECTRICAL -- no. 14 awg cond, black; both ends female quick-disconnect term., o/a length 36 in.	1014552-701	1
A25B1, A3A3D	. TERMINAL, QUICK DISCONNECT -- same as A25A1 u/w C3	937 200 001	2
C11 (A21A1 to A1H1B)	CABLE ASSY, POWER -- 3 cond cable; both ends 3-hermaphrodite contact connectors o/a length 5 ft	1014551-701	1
A21A1, A1H1B	. CONNECTOR, PLUG -- 3 hermaphrodite contacts; c/o the following individual items:		2
	.. SHELL, CONNECTOR -- nylon, black; accom 3 hermaphrodite contacts; ELCO 60-6501.3318-00-130	941 132 003	1
	.. CONTACT, ELECTRICAL -- fork type with one male and one female form one end and common solder term. with crimping tabs other end; accom no. 14 - 18 awg wire; ELCO 50-6501-0312	941 402 001	3
	. CABLE, POWER -- 3 cond no. 16 awg; Type SJ; rubber jacket; CORNISH WIRE 3303	940 075 001	5
C11 (A21A1 to A1H1B)	CABLE ASSY, POWER -- 3 cond cable; both ends 3-hermaphrodite contact connectors o/a length 5 ft	1014551-701	1
A21A1, A1H1B	. CONNECTOR, PLUG -- 3 hermaphrodite contacts; c/o the following individual items:		2
	.. SHELL, CONNECTOR -- nylon, black; accom 3 hermaphrodite contacts; ELCO 60-6501.3318-00-130	941 132 003	1
	.. CONTACT, ELECTRICAL -- fork type with one male and one female form one end and common solder term. with crimping tabs other end; accom no. 14 - 18 awg wire; ELCO 50-6501-0312	941 402 001	3
	. CABLE, POWER -- 3 cond no. 16 awg; Type SJ; rubber jacket; CORNISH WIRE 3303	940 075 001	5 ft
C12 (A21A2 to A4H1B)	CABLE ASSY, POWER -- reference only; refer to Table 6-4 for description and components	1014551-702	Ref

Table 4-1. (Cont)
DDP-516 Main Frame

Reference Designation	Description	3C Part No.	Qty Req
C13 (A3 to A21B1)	CABLE ASSY, POWER -- reference only; supplied with RP-61 power supply		Ref
C14 (A2 to AC Main)	CABLE ASSY, POWER		
C19 (A21A3 to B2H1B)	CABLE ASSY, POWER -- reference only; refer to Table 6-6 for description and components	1014551-703	Ref
A1H2B to A1Z2B	CABLE ASSY, SPECIAL PURPOSE -- 2 cond, no. 22 awg, cabled and covered w/insulating sleeve; one end of each conductor terminated w/female quick-disconnect term.; other end solder lug; o/a length 4 ft	2014215-701	1
A1H2B	. TERMINAL, QUICK DISCONNECT -- same as A4K1F u/w C2	937 200 002	2

Tables 4-2 and 4-3
(Pages 4-14 through 4-30) deleted.

Table 4-4.
4K and 8K Memory Parts List

Reference Designation	Description	3C Part No.	Qty Req	
			4K	8K
A4 Series	A4 UNIT -- 4092 (4K) WORDS, 16 BITS or 8192 (8K) WORDS, 16 BITS MEMORY			
A4A11, 3, 5, 7 A4A21, 3, 5, 7 A4A57 A4A67 A4B11, 3, 5, 7 A4B21, 3, 5, 7 A4B51, 3, 5, 7 A4B61, 3, 5, 7 A4C11, 3, 5, 7 A4C21, 3, 5, 7	μ-PAC DIGITAL MODULE--selection PAC	Model CM-006	34	34
A4A18, 28 A4B18, 28, 58, 68 A4C18, 28	μ-PAC DIGITAL MODULE--sense amplifier	Model CM-032	--	8
A4A18, 28 A4B18, 28, 58, 68 A4C18, 28	μ-PAC DIGITAL MODULE--sense amplifier	Model CM-033	8	--
A4A51*, 3, 5 A4A61*, 3, 5	μ-PAC DIGITAL MODULE--selection PAC Note: ref. desig. marked with asterisk (*) required on 8K only	Model CM-106	4	6
A4A58	μ-PAC DIGITAL MODULE--component PAC	Model CM-075	1	1
A4C51 A4C61	μ-PAC DIGITAL MODULE--timing distribution	Model CM-003	2	2
A4C52 A4C63, 5, 7	μ-PAC DIGITAL MODULE--power amplifier	Model PA-335	4	4
A4C53 A4C64	μ-PAC DIGITAL MODULE--transfer gate	Model TG-335	2	2
A4C62	μ-PAC DIGITAL MODULE--NAND gate Type 2	Model DL-335	1	1
A4	MEMORY DRAWER ASSY--c/o one PAC connector plane, core stack, resistor group, cooling fans, swinging/locking mechanism and associated parts; incl mtg provisions for additional PAC connector planes for memory expansion or option use	6013020-701 6013020-705	1 --	-- 1
A4N through W	. INTEGRATED CORE STACK ASSY--4096 words, 16 bits/word; incl core planes, integrated circuit modules and associated parts	942 503 004	1	--
	.. INTEGRATED CIRCUIT--diode matrix; designed to mount flat on printed wiring board; 7 flat wire radial term. each side; o/a dim. 0.065 in. thk by 0.125 in. w by 0.250 in. lg excl terminals	Type F-08	32	--
A4N through W	. INTEGRATED CORE STACK ASSY--8192 words, 16 bits/word; incl core planes, integrated circuit modules and associated parts	942 503 011	--	1
	.. INTEGRATED CIRCUIT--same as u/w 4K core stack	Type F-08	--	32

Table 4-4. (Cont)
4K and 8K Memory Parts List

Reference Designation	Description	3C Part No.	Qty Req	
			4K	8K
A4A/B/C1, 2, 5, 6	. CONNECTOR PLANE ASSY--c/o two 2x3 modules (12 connector blocks of 8 connectors each), framework and associated parts; factory repairable only	4013007-701	1	1
A4A1, 2, 5, 6 A4B1, 2, 5, 6 A4C1, 2	. DECOUPLING MODULE--c/o two 3.3 mf capacitors epoxy encapsulated; 3 pin term.; o/a dim. 0.240 in. w by 0.340 in. h by 1.960 in. lg excl term.	2011516-701	10	10
A4C5, 6	. DECOUPLING MODULE--c/o two 20 mf capacitors epoxy encapsulated; 3 pin term.; o/a dim. 0.240 in. w by 0.340 in. h by 1.960 in. lg excl term.	2011516-702	2	2
A4G2	. RESISTOR ASSY--c/o 36 resistors, 2 capacitors and associated parts mtd on alum. plate	3013008-701	1	1
A4G2A1, 10	.. CAPACITOR, MICA--510 pf, 5%, 100 vdcw; radial leads; ELMENCO DM15F511J100wv	930 011 146	2	2
A4G2B1 through 18 A4G2D1 through 18	.. RESISTOR, WIREWOUND--53 ohms, 1%, 5w; non-inductive; silicone coating; DALE NS5-53-1PCT	932 215 009	36	36
A4H	. FAN ASSY, AXIAL--see A1H, Table 6-1 for description and components	4011031-705	1	
A4K	. CONNECTOR ASSY--see A1K, Table 6-1 for description and components	3014214-701	1	
A4Z	. FAN ASSY, AXIAL--see A1Z, Table 6-1 for description and components	4011031-701	1	
u/w A4Z	. FILTER, AIR--see Table 6-1 for description	911 003 004	1	
	. LOCKING MECHANISM ASSY--see Table 6-1 for description	2011121-701	1	
	. CABLE, WIRE--see Table 6-1 for description	1011538-001	1	
	. PULLEY ASSY--see Table 6-1 for description	2011304-701	2	
	. HANDLE ASSY--see Table 6-1 for description	3011212-701	1	
C7 (A4K to A3)	CABLE ASSY, SPECIAL PURPOSE--c/o seven No. 14 AWG conductors cabled and covered w/insulating sleeve; each conductor terminated both ends e/female quick-disconnect term.; o/a length 80 in.	1014553-701	1	1
A3A1A, B, D, E, F A3A10D, E	. TERMINAL, QUICK DISCONNECT--female; accom 1/4 in. w by 0.032 in. thk blade male contact; crimp type ferrule for No. 14-No. 18 AWG wire; THOMAS and BETTS RB250	937 200 001	7	7
A4K1A through G	. TERMINAL, QUICK DISCONNECT--female; accom 1/4 in. w by 0.032 in. thk blade male contact; crimp lype ferrule for No. 14-No. 16 AWG wire; THOMAS and BETTS B250	937 200 003	7	7
A4C68 to A1E58	CABLE ASSY, SPECIAL PURPOSE--32-pairs cable terminated each end w/printed wiring assy; o/a length 56 in.	1014997-701	1	1

Table 4-4. (Cont)
4K and 8K Memory Parts List

Reference Designation	Description	3C Part No.	Qty Req	
			4K	8K
A4C68	. PRINTED WIRING ASSY--c/o board, component and associated parts	2013767-701	1	1
	.. PRINTED WIRING BOARD--0.047 in. thk epoxy glass; copper clad both sides	2013767, Items 1-4	1	1
A4C68-C1	.. CAPACITOR, PLASTIC--0.033 mf, 20%, 50 vdcw; MIDWEC CO. 3XF-.033-20%	930 313 016	1	1
A1E58	. PRINTED WIRING ASSY--c/o board, components and associated parts	2014995-701	1	1
	.. PRINTED WIRING BOARD--0.047 in. thk epoxy glass; copper clad both sides	2014995, Items 1-5	1	1
A1E58-C1	.. CAPACITOR, PLASTIC, same as A4C68-C1	930 313 016	1	1
A1E58-R1 through R32	.. RESISTOR, COMPOSITION--20 ohms, 5%, 1/8w; MIL Type RC05GF200J	932 010 008	32	32
	. CABLE, SPECIAL PURPOSE--32 pairs, No. 28 AWG; plastic jacket	940 359 001	56 in.	56 in.
	. PLATE, CLAMPING--cres; 0.047 in. thk; four 2-56 thd mtg holes	2013626-001	2	2
	. CLAMP--half loop; cres; 0.032 in. thk; 1/4 in. w; two 0.110 in. dia mtg holes	1013623-001	2	2
A4C67 to A1F61	CABLE ASSY, SPECIAL PURPOSE--32-pairs cable terminated each end w/printed wiring assembly; o/a length 52 in.	1014997-703	1	1
A4C67	. PRINTED WIRING ASSY--same as A4C68	2013767-701	1	1
A1F61	. PRINTED WIRING ASSY--c/o board, components and associated parts	2014995-702	1	1
A1F61-C1	.. CAPACITOR, PLASTIC--same as A4C68-C1	930 313 016	1	1
A1F61-R1 through R14	.. RESISTOR, COMPOSITION--62 ohms, 5%, 1/8w; MIL Type RC05GF620J	932 010 020	14	14
	. CABLE, SPECIAL PURPOSE--same as u/w A4C68 to A1E58	940 359 001	52 in.	52 in.
	. PLATE, CLAMPING--same as u/w A4C68 to A1E58	2013626-001	2	2
	. CLAMP--same as u/w A4C68 to A1E58	1013623-001	2	2
C12 (A4H1B to A21A2)	CABLE ASSY, POWER--same as part no. 1014551-701 except o/a length 70 in.; see Table 6-1 for 1014551-701 description and components	1014551-702	1	1
A4H2B to A4Z2B	CABLE ASSY, SPECIAL PURPOSE--see Table 6-1 for description and components	2014215-701	1	1

Table 4-5.
12K and 16K Memory Parts List

Reference Designation	Description	3C Part No.	Qty Req	
			12K	16K
A4 and A5 Series	A4/A5 UNIT--12276 (12K) WORDS, 16 BITS or 16384 (16K) WORDS, 16 BITS MEMORY			
A4/A5A11,3,5,7 A4/A5A21,3,5,7 A4/A5A57 A4/A5A67 A4/A5B11,3,5,7 A4/A5B21,3,5,7 A4/A5B51,3,5,7 A4/A5B61,3,5,7 A4/A5C11,3,5,7 A4/A5C21,3,5,7	μ-PAC DIGITAL MODULE--sclection PAC	Model CM-006	68	68
A4A18,28 A4B18,28,58,68 A4C18,28 A5A18*,28* A5B18*,28*,58*,68* A5C18*,28*	μ-PAC DIGITAL MODULE--sense amplifier Note: rcf. desig. marked with asterisk (*) required on 16K only	Model CM-032	8	16
A4A51,3,5 A4A61,3,5 A5A51*,3,5 A5A61*,3,5	μ-PAC DIGITAL MODULE--selection PAC Note: ref. desig. marked with asterisk (*) required on 16K only	Model CM-106	10	12
A4A58 A5A58	μ-PAC DIGITAL MODULE--component PAC	Model CM-075	2	2
A4C51,61 A5C51,61	μ-PAC DIGITAL MODULE--timing distribution	Model CM-003	4	4
A4C52,63,65,67 A5C52,63,65,67	μ-PAC DIGITAL MODULE--power amplifier	Model PA-335	8	8
A4C53,64 A5C53,64	μ-PAC DIGITAL MODULE--transfer gate	Model TG-335	4	4
A4C62 A5C62	μ-PAC DIGITAL MODULE--NAND gate Type 2	Model DL-335	2	2
A5A18,28 A5B18,28,58,68 A5C18,28	μ-PAC DIGITAL MODULE--sense amplifier	Model CM-033	8	--
A4/A5	MEMORY DRAWER ASSY--c/o two PAC connector planes, core stacks, resistor groups, cooling fans, swinging/locking mechanism and associated parts	6013020-703 6013020-707	1 --	-- 1
A4N through W A5N through W	. INTEGRATED CORE STACK ASSY--8192 words; see Table 6-4 for description and components	942 503 011	1	2
A5N through W	. INTEGRATED CORE STACK ASSY--4096 words; see Table 6-4 for description and components	942 503 008	1	--
A4A/B/C1,2,5,6 A5A/B/C1,2,5,6	. CONNECTOR PLANE ASSY--see Table 6-4 for description	4013007-701	2	2

Table 4-5. (Cont)
12K and 16K Memory Parts List

Reference Designation	Description	3C Part No.	Qty Req	
			12K	16K
A4/A5A1, 2, 5, 6 A4/A5B1, 2, 5, 6 A4/A5C1, 2	. DECOUPLING MODULE--see Table 6-4 for description	2011516-701	20	20
A4C5, 6 A5C5, 6	. DECOUPLING MODULE--see Table 6-4 for description	2011516-702	4	4
A4G2 A5G4	. RESISTOR ASSY--see Table 6-4 for description and components	3013008-701	2	2
A4H	. FAN ASSY, AXIAL--see A1H, Table 6-1 for description and components	4011031-705	1	1
A4K	. CONNECTOR ASSY--see A1K, Table 6-1 for description and components	3014214-701	1	1
A4Z	. FAN ASSY, AXIAL--see A1Z, Table 6-1 for description and components	4011031-701	1	1
u/w A4Z	. FILTER, AIR--see Table 6-1 for description	911 003 004	1	1
	. LOCKING MECHANISM ASSY--see Table 6-1 for description	2011121-701	1	1
	. CABLE, WIRE--see Table 6-1 for description	1011538-001	1	1
	. PULLEY ASSY--see Table 6-1 for description	2011304-701	2	2
	. HANDLE ASSY--see Table 6-1 for description	3011212-701	1	1
C8 (A4K to A3)	CABLE ASSY, SPECIAL PURPOSE--c/o twelve No. 14 AWG conductors cabled and covered w/insulating sleeve; each conductor terminated both ends w/female quick-disconnect term.; o/a length 80 in.	1014553-702	1	1
A3A1A, B, C, D, E F A3A10D, E A3A2A, B, E, F	. TERMINAL, QUICK DISCONNECT--female; accom 1/4 in. w by 0.032 in. thk blade male contact; crimp type ferrule for No. 14-18 AWG wire; THOMAS and BETTS RB250	937 200 001	12	12
A4K1A through M	. TERMINAL, QUICK DISCONNECT--female; accom 1/4 in. w by 0.032 in. thk blade male contact; crimp type ferrule for No. 14-16 AWG wire; THOMAS and BETTS B250	937 200 003	12	12
A4C68 to A1E58	CABLE ASSY, SPECIAL PURPOSE--see Table 6-4 for description and components	1014997-701	1	1
A4C67 to A1F61	CABLE ASSY, SPECIAL PURPOSE--see Table 6-4 for description and components	1014997-703	1	1
A5C67 to A1F58	CABLE ASSY, SPECIAL PURPOSE--same as part no. 1014997-703 except o/a length 46 in.; see Table 6-4 for 1014997-703 description and components	1014997-704	1	1
A4B68 to A5C68	CABLE ASSY, SPECIAL PURPOSE--32-pairs cable terminated each end w/printed wiring board; o/a length 2 ft	1013826-701	1	1

Table 4-5. (Cont)
12K and 16K Memory Parts List

Reference Designation	Description	3C Part No.	Qty Req	
			12K	16K
A4B68 A5C68	. PRINTED WIRING BOARD--μ-PAC configuration w/o components; incl cable clamp, clamping bar and plate	2013625-701	2	2
	. CABLE, SPECIAL PURPOSE--32 pairs, No. 28 AWG; plastic jacket	940 359 001	2 ft	2 ft
C12 (A4H1B to A21A2)	CABLE ASSY, POWER--same as part no. 1014551-701 except o/a length 70 in.; see Table 6-1 for 1014551-701 description and components	1014551-702	1	1
A4H2B to A4Z2B	CABLE ASSY, SPECIAL PURPOSE--see Table 6-1 for description and components	2014215-701	1	1

Table 4-6.
24K and 32K Memory Parts List

Reference Designation	Description	3C Part No.	Qty Req	
			24K	32K
	A4/A5 and B2 UNITS -- 24576 (24K) WORDS 16 BITS MEMORY or A4/A5 and B2/B1 UNITS -- 32768 (32K) WORDS 16 BITS MEMORY Note: A4/A5 Unit located in Main Frame B2/B1 Unit located in Option Equipment Cabinet B1 ref. desig. items are used only on 32K memory μ-PAC COMPLEMENT (Prefix all ref. desig. with A4, A5, B2 and B1 for complete system designation)			
A11, 3, 5, 7 A21, 3, 5, 7 A57 A67 B11, 3, 5, 7 B21, 3, 5, 7 B51, 3, 5, 7 B61, 3, 5, 7 C11, 3, 5, 7 C21, 3, 5, 7	μ-PAC DIGITAL MODULE--selection PAC	Model CM-006	102	136
A18, 28 B18, 28, 58, 68 C18, 28	μ-PAC DIGITAL MODULE--sense amplifier	Model CM-032	24	32
A51, 3, 5 A61, 3, 5	μ-PAC DIGITAL MODULE--selection PAC	Model CM-106	18	24
A58	μ-PAC DIGITAL MODULE--component PAC	Model CM-075	3	4
C51 C61	μ-PAC DIGITAL MODULE--timing distribution	Model CM-003	6	8
C52 C63, 5, 7	μ-PAC DIGITAL MODULE--power amplifier	Model PA-335	12	16
C53 C64	μ-PAC DIGITAL MODULE--transfer gate	Model TG-335	6	8
C62	μ-PAC DIGITAL MODULE--NAND gate Type 2	Model DL-335	3	4
A4/A5 B2/B1	MEMORY DRAWER ASSY--c/o two PAC connector planes, core stacks, resistor groups, cooling fans, swinging/locking mechanism and associated parts (Note: B2/B1 used only on 32K)	6013020-707	1	2
B2	MEMORY DRAWER ASSY--c/o one PAC connector plane, core stack, resistor group, cooling fans, swinging/locking mechanism and associated parts; incl mtg provision for additional PAC connector planes for memory expansion or option use Note: the top figure in the 24K qty reqd column is the qty for 6013020-707, the bottom figure is the qty for 6013020-705.	6013020-705	1	--

Table 4-6. (Cont)
24K and 32K Memory Parts List

Reference Designation	Description	3C Part No.	Qty Req 24K	Qty Req 32K
A4N through W A5N through W B2N through W B1N through W	. INTEGRATED CORE STACK ASSY--8192 words; see Table 6-4 for description and components	942 503 011	2 1	2
A4A/B/C1, 2, 5, 6 A5A/B/C1, 2, 5, 6 B2A/B/C1, 2, 5, 6 B1A/B/C1, 2, 5, 6	. CONNECTOR PLANE ASSY--see Table 6-4 for description	4013007-701	2 1	2
A4/A5A1, 2, 5, 6 A4/A5B1, 2, 5, 6 A4/A5C1, 2 B2A1, 2, 5, 6 B2B1, 2, 5, 6 B2C1, 2 B1A1, 2, 5, 6 B1B1, 2, 5, 6 B1C1, 2	. DECOUPLING MODULE--see Table 6-4 for description	2011516-701	20 10	20
A4C5, 6 A5C5, 6 B2C5, 6 B1C5, 6	. DECOUPLING MODULE--see Table 6-4 for description	2011516-702	4 2	4
A4G2 A5G4 B2G2 B1G4	. RESISTOR ASSY--see Table 6-4 for description and components	3013008-701	2 1	2
A4H B2H	. FAN ASSY, AXIAL--see A1H, Table 6-1 for description and components	4011031-705	1	1
A4K B2K	. CONNECTOR ASSY--see A1K, Table 6-1 for description and components	3014214-701	1 1	1
A4Z B2Z	. FAN ASSY, AXIAL--see A1Z, Table 6-1 for description and components	4011031-701	1 1	1
u/w A4Z, B2Z	. FILTER, AIR--see Table 6-1 for description	911 003 004	1 1	1
	. LOCKING MECHANISM ASSY--see Table 6-1 for description	2011121-701	1 1	1
	. CABLE, WIRE--see Table 6-1 for description	1011538-001	1 1	1
	. PULLEY ASSY--see Table 6-1 for description	2011304-701	2 2	2
	. HANDLE ASSY--see Table 6-1 for description	3011212-701	1 1	1
C8 (A4K to A3) C10 (B2K to A3)	CABLE ASSY, SPECIAL PURPOSE--see Table 6-5 for description and components; C10 used on 32K only	1014553-702	1	2
C9 (B2K to A3)	CABLE ASSY, SPECIAL PURPOSE--same as part no. 1014553-701 except o/a length 98 in.; see Table 6-4 for 1014553-701 description and components	1014553-703	1	--

Table 4-6. (Cont)
24K and 32K Memory Parts List

Reference Designation	Description	3C Part No.	Qty Req	
			24K	32K
A4C68 to A1E58	CABLE ASSY, SPECIAL PURPOSE--see Table 6-4 for description and components	1014997-701	1	1
A4C67 to A1F61	CABLE ASSY, SPECIAL PURPOSE--see Table 6-4 for description and components	1014997-703	1	1
A5C67 to A1F58	CABLE ASSY, SPECIAL PURPOSE--same as part no. 1014997-703 except o/a length 46 in.; see Table 6-4 for 1014997-703 description and components	1014997-704	1	1
B2C68 to A1E51	CABLE ASSY, SPECIAL PURPOSE--same as part no. 1014997-701 except o/a length 84 in.; see Table 6-4 for 1014997-701 description and components	1014997-702	1	1
B2C67 to A1F51	CABLE ASSY, SPECIAL PURPOSE--same as part no. 1014997-703 except o/a length 80 in.; see Table 6-4 for 1014997-703 description and components	1014997-705	1	1
B1C67 to A1F48	CABLE ASSY, SPECIAL PURPOSE--same as part no. 1014997-703 except o/a length 74 in.; see Table 6-4 for 1014997-703 description and components	1014997-706	--	1
A4B68 to A5C68 B2B68 to B1C68	CABLE ASSY, SPECIAL PURPOSE--see Table 6-5 for description and components; B2B68 to B1C68 used on 32K only	1013826-701	1	2
C11 (A4H1B to A21A2)	CABLE ASSY, POWER--same as part no. 1014551-701 except o/a length 70 in.; see Table 6-1 for 1014551-701 description and components	1014551-702	1	1
C19 (B2H1B to A21A3)	CABLE ASSY, POWER--same as part no. 1014551-701 except o/a length 90 in.; see Table 6-1 for 1014551-701 description and components	1014551-703	1	1
A4B2B to A4Z2B B2B2B to B2Z2B	CABLE ASSY, SPECIAL PURPOSE--see Table 6-1 for description and components	2014215-701	2	2

APPENDIX
μ-PAC DESCRIPTIONS

This appendix contains descriptions of the majority of special μ-PAC integrated circuit modules which are used in the basic DDP-516 computer and its applicable options. Specific limited use standard and special μ-PACs used in the options are described in the respective option manual.

The μ-PAC descriptions given here are preceded by a general description of the basic microcircuit characteristics.

The μ-PAC integrated circuit modules described are listed below.

The following standard μ-PACs are described in the instruction manual for μ-PAC Integrated Circuit Modules, Document No. 70130071369.

No.	No.
DC-335	LC-335
DI-335	OD-335
DL-335	PA-335
DM-335	PA-336
DN-335	ST-335
FF-335	TG-335

MICROCIRCUIT CHARACTERISTICS

INTRODUCTION

This section contains general specifications for the μ-PAC digital module line and detailed technical data on the four basic integrated circuit types used throughout the product line for digital logic functions.

GENERAL μ-PAC SPECIFICATIONS

All performance specifications listed below are guaranteed minimums based on worst-case tolerances. Actual performance will invariably exceed these guaranteed minimums. The following specifications apply to all μ-PAC types. Any exceptions are listed in the individual specifications.

Input Switching Thresholds (Refer to Figure A-1.)

a. NAND gate and flip-flop dc inputs
   Active: +1.1v(min), +1.35v (typ)
   Passive: +3.0v(max), +1.55v (typ)

b. Power Amplifier and flip-flop clock and control inputs
   Active: +1.2v(min), +1.6v (typ)
   Passive: +3.0v(min), +1.8v (typ)

Output Logic Levels (Guaranteed for all circuit types)

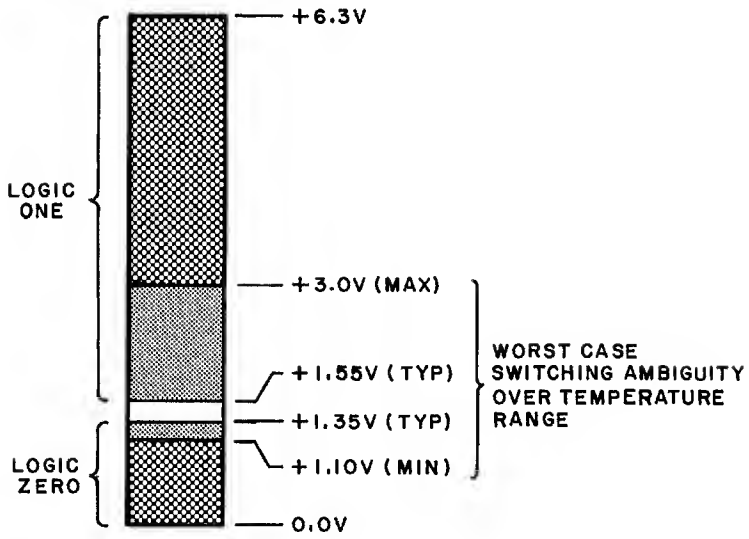
Passive: +4.0v (min) to +6.3v (max)
Active: 0v to 0.35v (max)

When referring to the outputs of circuits, the terms "set" and "reset" denote level outputs and "assertion" and "negation" denote pulse outputs. Flip-flops produce level outputs; one-shots and clocks produce pulse outputs.

Frequency Range (DC to 5 MC)

One common way of describing the speed of a digital circuit is to state the highest frequency square or rectangular wave that can be applied to the input of a circuit and still reliably produce a specified output. Applied to a flip-flop, this method specifies the highest toggling or complementing rate possible; and for a gate, an input discrimination capability dependent on its circuit delay. Of course, these circuits would be driving light loads. Such

a. NAND GATE AND FLIP-FLOP DC INPUTS



b. POWER AMPLIFIER AND FLIP-FLOP CLOCK AND CONTROL INPUTS

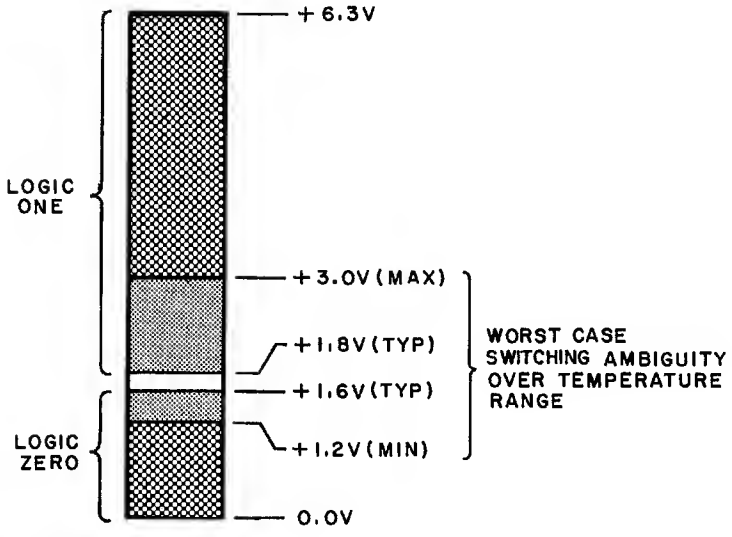


Figure A-1. Switching Thresholds

an approach is often misleading and unusable for the systems designer. When many of the same types of circuits are used in a system, the system capability or operating frequency depends on accumulated circuit delays. There must also be a reasonable fanout from any logic circuit; otherwise extra circuits would be needed in parallel or series in order to drive a moderate amount of logic. Rise and fall times of individual circuits are primarily meaningful only to the extent that they affect circuit delay.

An alternate measure of the efficiency of a system is the number of stages or levels of logic through which a signal can pass during a clock period. Honeywell, Inc. has chosen to specify the μ-PAC digital circuit line from this standpoint of system operating frequency. The standard flip-flop can actually toggle at 10 mc, but is specified as having an operating frequency of 5 mc. The flip-flop requires only 40 nsec set up time before triggering. At a 5 mc clock rate, 160 nsec is available for going through logic, enough time for the initial clocked flip-flop delay plus three gate delays. All logic circuits in the chain have a fanout of eight at this frequency.

Temperature Range

Operating ambient (System):	$0^{\circ}C$ to $+55^{\circ}C$
Storage:	$-65^{\circ}C$ to $+155^{\circ}C$

Power Supplies

a. Positive Voltage

Nominal:	+6.0v
Operating range:	+5.1v to +6.3v
Absolute maximum rating:	+8.0v

b. Negative voltage (used on hybrid modules only)

Nominal:	-6.0v
Operating range:	-5.7v to -6.3v
Absolute maximum rating:	-8.0v

Absolute maximum voltage ratings cannot be exceeded without the risk of circuit damage.

Loading Rules

Loading specifications for μ-PACs are expressed in terms of "unit loads," both for input loading and output drive capability. The unit load concept simplifies calculation of total loading imposed on a driving stage that is fanned out to a number of different circuit types. For μ=PAC, a unit load is defined as the power required to drive the input circuit of a NAND gate (nominally 1.6 ma dc). Unit load ratings apply to the ground signal condition at a gate input. (Gates require no input power when all inputs are passive or are not connected.)

Current Requirements

Current requirements are listed in the specifications for each individual μ-PAC. The requirements are calculated on a nominal worst-case basis, in which the circuit inputs are assumed to be in the condition capable of causing the maximum current drain for a particular voltage. The nominal worst-case is selected instead of the extreme worst-case to provide a more realistic figure for power requirements and therefore permit more equipment to be driven by a power supply. Since it is very unlikely that all gates in a system would be on at the same time, the nominal worst-case calculations provide a considerable safety factor.

The current specifications include only the current used in the specific μ-PAC and do not include the current going to external loads. Since the input load current is included in the specification, total system current requirements can be calculated by adding the rated currents for all μ-PACs in the system.

Worst Case Delays

Worst-case delays are specified over the full temperature range and under loading conditions which result in the longest propagation delay. (Eight dc gate loads are assumed for turn-on and one active dc gate load is assumed for turn-off.) For a gating circuit, the delay is specified as the average of the turn-on and turn-off delays. The total capacitance driven under the specified worst-case condition is 15 pf of wiring capacitance plus the capacitance accumulated in a μ-BLOC system when driving eight unit loads. This capacitance may be present during turn-off as well as turn-on, since it is possible to fan out to eight unit loads and yet have only one gate active. (The other seven loads may be inhibited by inputs at ground.) The effect of additional wiring capacitance on gate delays is discussed under Typical Delay Characteristics.

The preceding conditions apply to all gate and flip-flop circuits. Power amplifier delay specifications assume the condition of driving 25 active dc gate loads plus a total of 250 pf of capacitance.

Typical Delay Characteristics

The curves in Figure A-2 show typical circuit delays of the basic NAND gate, plotted against variations in temperature, system wiring capacitance, and dc and capacitive loading conditions. For example, the "5 loads, 1 active" curve shows the delay characteristic of a gate output that fans out to five gates, four of which are inhibited by logic ZERO signals on other inputs. Connector, printed circuit, and input capacitance when fanning out to 5 unit loads are taken into consideration. The worst-case condition is also plotted. This is the "8 loads, 1 active" curve, where 1 active load is being driven from an output that fans out to 8 unit loads. In this situation, the maximum stray capacitance is being driven by the minimum charging current, resulting in longer turn-off delays.

Although the curves are plotted beyond 40 picofarads of additional wiring capacitance, that amount of wiring capacitance is unlikely to appear on any output in a μ-BLOC

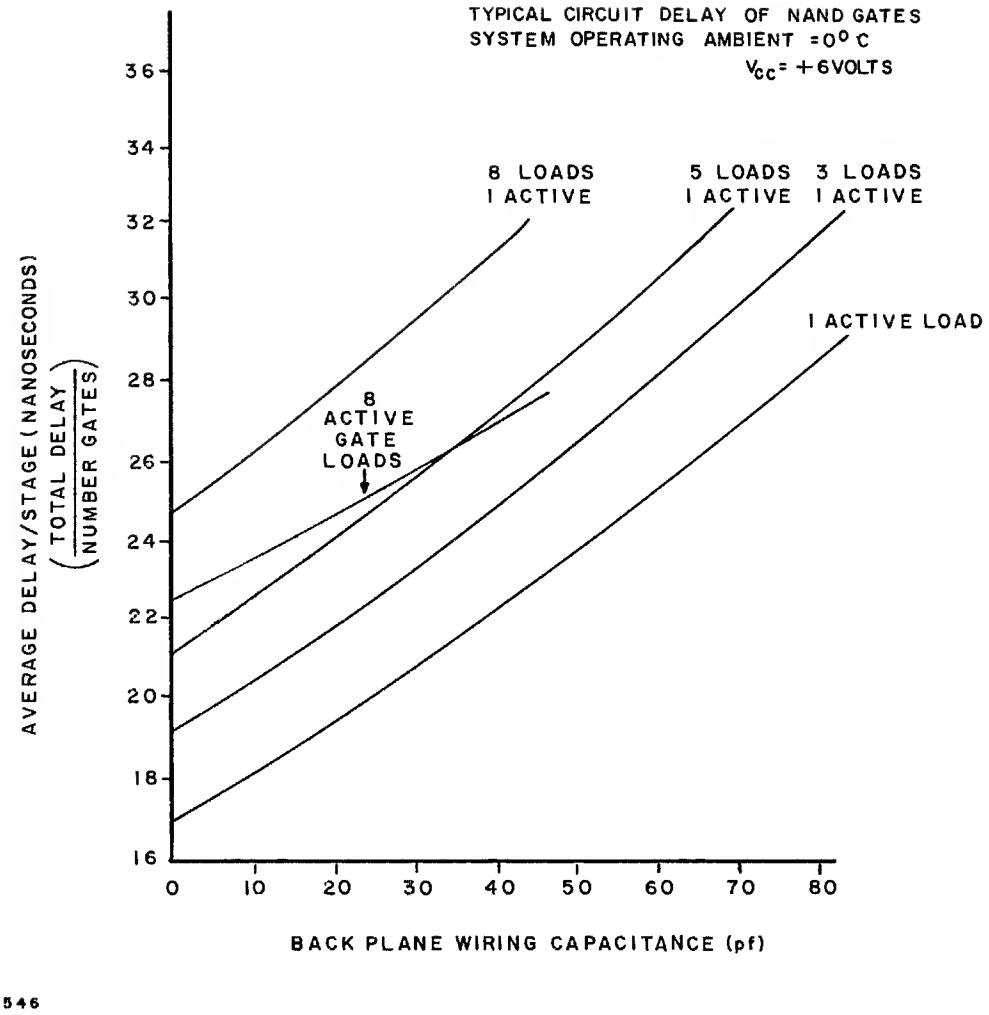
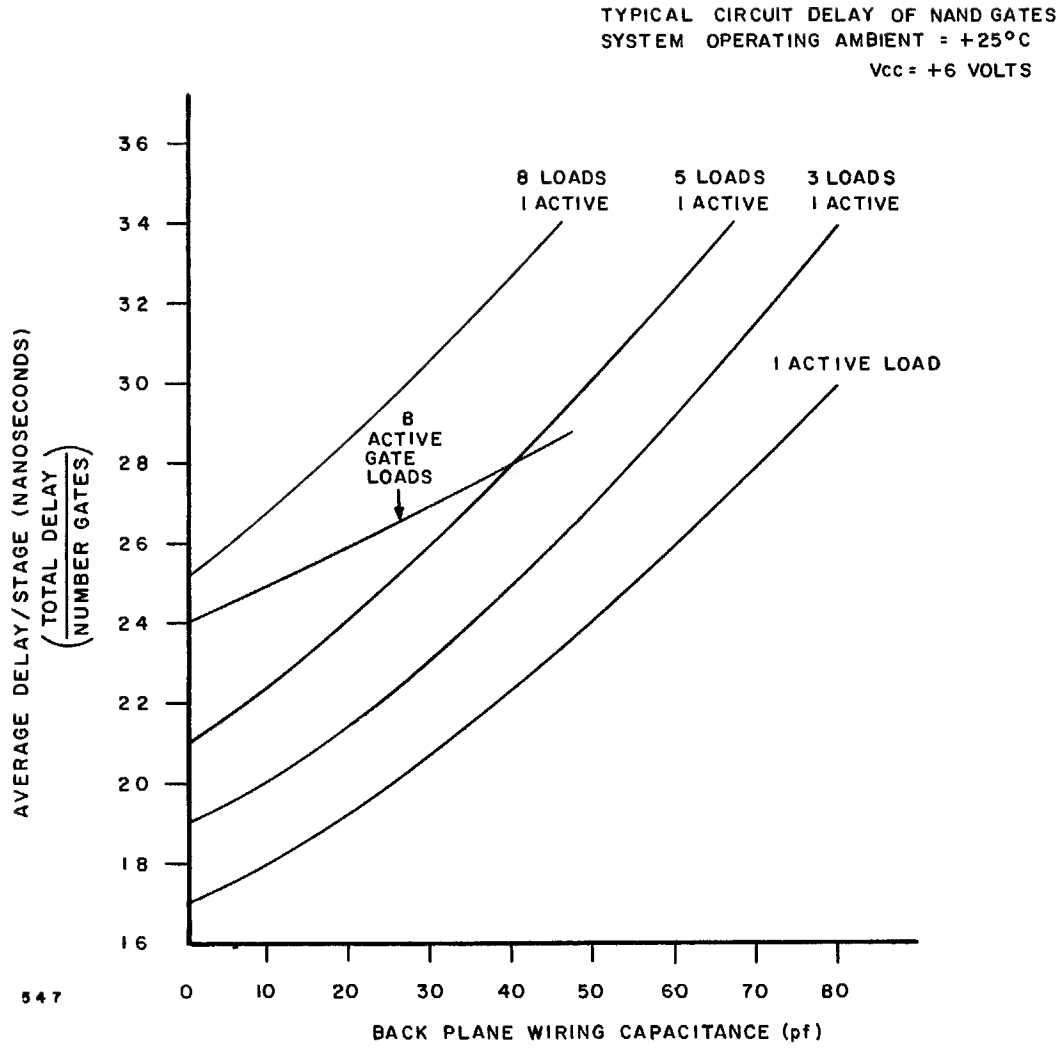


Figure A-2. Typical NAND Gate Circuit Delays (Sheet 1 of 3)



A-2. Typical NAND Gate Circuit Delays (Sheet 2 of 3)

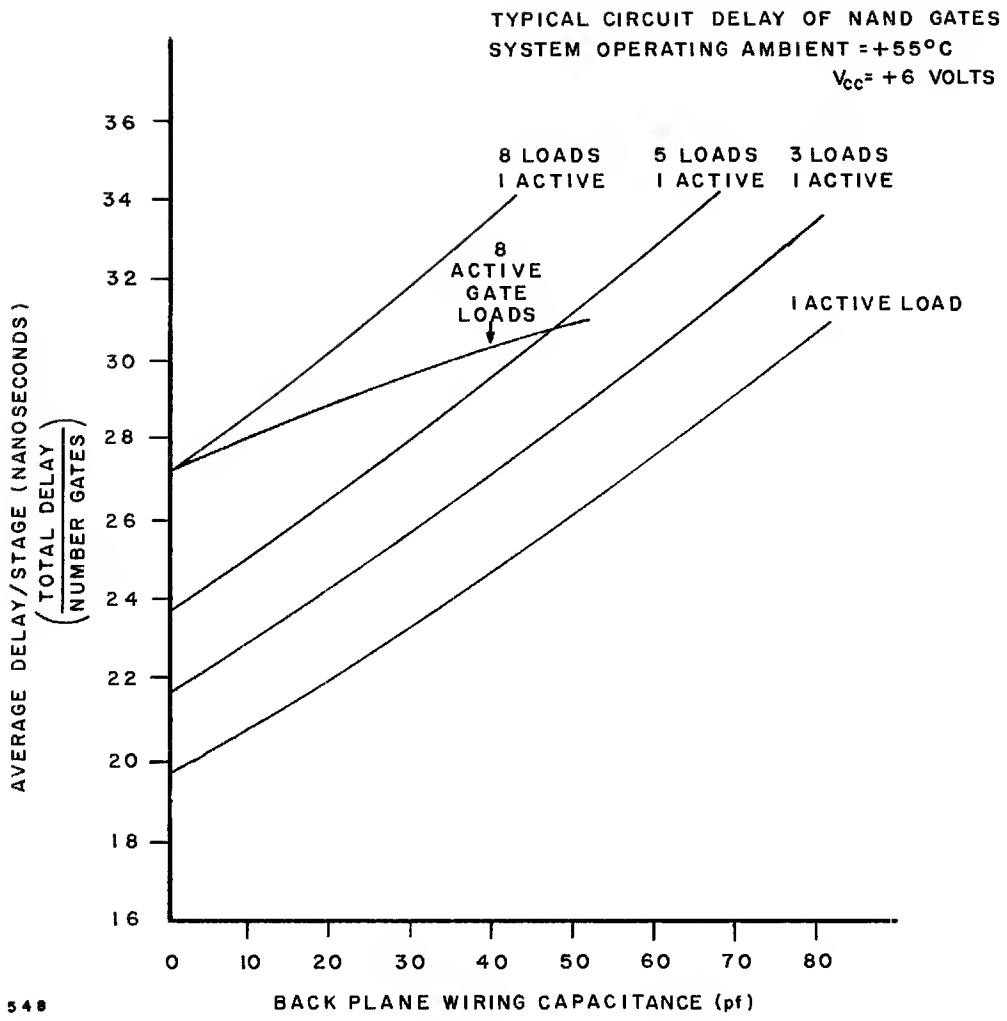


Figure A-2. Typical NAND Gate Circuit Delays (Sheet 3 of 3)

system. The stray wiring capacitance will vary between 6 and 12 picrofarads per foot, depending on the system wiring density. Due to the relatively small size of a μ-BLOC the wiring runs are minimized.

Typical Waveform Characteristics

The waveforms shown in Figure A-3 are typical of a Model MC-335 clock driving a flip-flop, power amplifier, and two NAND gates in a series chain, with all logic elements operating at one-half their rated full load.

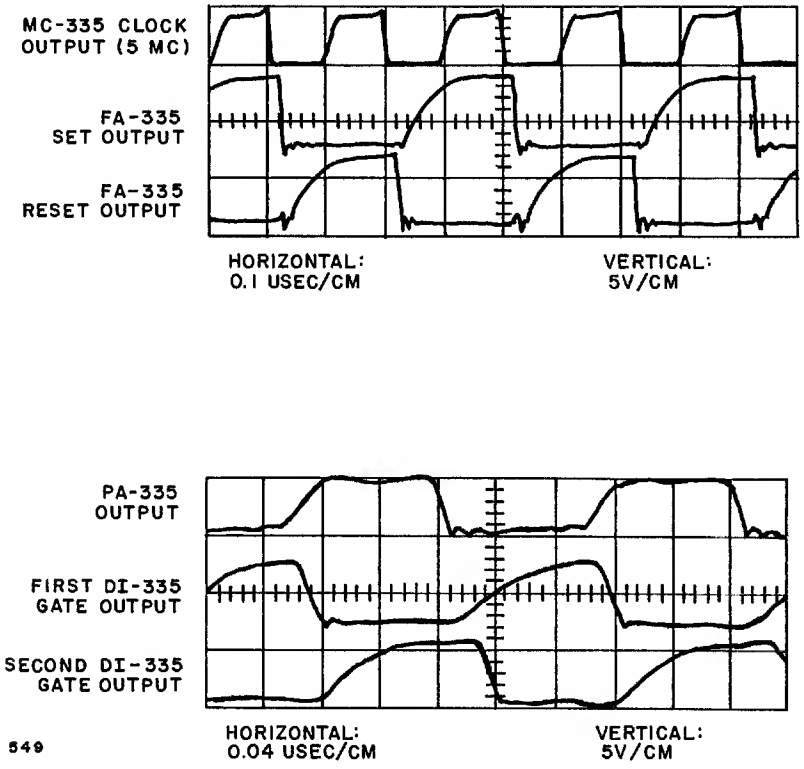


Figure A-3. Typical μ-PAC Waveforms

NAND GATE F-01 AND F-02 CHARACTERISTICS

Basic NAND Circuit

The standard μ-PAC NAND gate is a grounded-emitter, inverter amplifier. All inputs are diode-buffered, and the output is either the voltage of a saturated transistor or the supply voltage. Accidental grounding of the output will not damage the circuit.

The gate performs the NAND function with conventional positive logic (+6v = ONE, 0v = ZERO). For negative logic, the gate performs the NOR function. (See Figure A-4.)

When all inputs are passive (+6v) or open, the output transistor is turned on, and the output is active (ground). If any input is at ground, the transistor is turned off, and the output is passive (the supply voltage, +6v).

F-01 and F-02 NAND Microcircuits

In order to obtain maximum logic flexibility two types of NAND gate microcircuits are used, the F-01 dual NAND gate and the F-02 quad NAND gate. The two NAND gate types have similar specifications and differ only in logic capability. (See Figure A-5.)

The F-01 dual NAND gate microcircuit contains two 3-input gates, each with an input node and a separate load resistor. The number of inputs to any gate can be expanded by tying the node of a gate to the node of a diode cluster. Outputs of gates with separate load resistors can be tied together as shown in Figure A-6, to perform the AND-OR-INVERT function without loss of output drive capability.

The F-02 quad NAND gate microcircuit contains four 2-input NAND gates. Pairs of gates can be wired back to back to form a dc set-reset flip-flop.

Loading

Input Loading:	1 unit load
Output Drive Capability:	8 unit loads (capable of also driving 75 pf total capacitance with delays as specified)

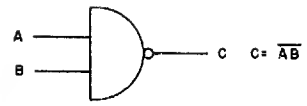
Outputs of gates with separate load resistors can be tied together to 1 load resistor with no loss in output drive capability.

Fan-In Expansion Using Nodes

12 at 5 mc

24 at 1 mc

Maximum fan-in is limited primarily by the maximum tolerable delays. The average propagation delay increases 3 nsec with each diode cluster that is tied to a node. The wire between nodes should be kept as short as possible by locating the PACs as close as possible to one another.



A. LOGIC FUNCTION

B. TRUTH TABLE

INPUT 1	INPUT 2	OUTPUT
0	0	1
0	1	1
1	0	1
1	1	0

0 = GROUND
1 = +6V

560

Figure A-4. Basic NAND Gate Logic

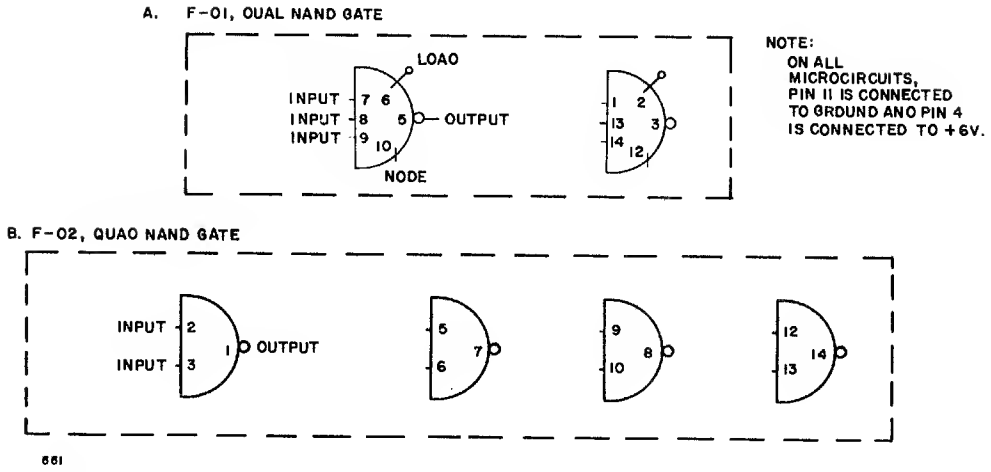


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Figure A-5. Types F-01 and F-02 NAND Gate Equivalent Logic Symbols

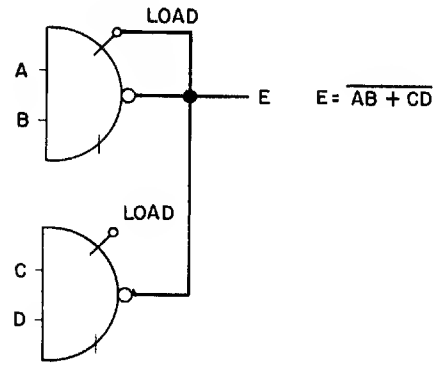

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Figure A-6. Paralleled NAND Gates with Common Load Resistors

Circuit Delay

(Measured at the +1.5v level, and averaged over 2 stages)

24 nsec (typ)

30 nsec (max)

The maximum delay specifications stated in the detailed μ-PAC descriptions are based on worst-case loading conditions for both turn on and turn off. Typical delays are based on one-half maximum rated loading.

Load Resistors in Parallel

When the outputs of two type F-02 NAND gates are tied together, the structure has a fanout capability of 4 unit loads (two load resistors are in parallel). When the outputs of three type F-02 NAND gates are tied together, the structure has a fanout of 1 unit load (three load resistors are in parallel).

Load Resistors in Parallel	Output Drive Capability
1	8
2	4
3	1

Paralleling Outputs with One Load Resistor

The maximum number of type F-01 NAND gate collector outputs that can be connected to one load resistor is limited by the maximum tolerable delay. The average propagation delay increased 3 nsec for each additional collector output that is jumpered through a connector to a standard output.

TYPE F-03 POWER AMPLIFIER CHARACTERISTICS

The type F-03 power amplifier microcircuit has two 3-input inverter amplifiers with nodes for input gating expansion. (See Figure A-7.) The power amplifier circuit is logically equivalent to the NAND gate but has about three times the output drive capability. It has a short circuit protection network such that accidental grounding of the output will not damage the circuit.

Input Loading

2 unit loads

Output Drive Capability

25 unit loads (capable of also driving 250 pf total capacitance with delays as specified)

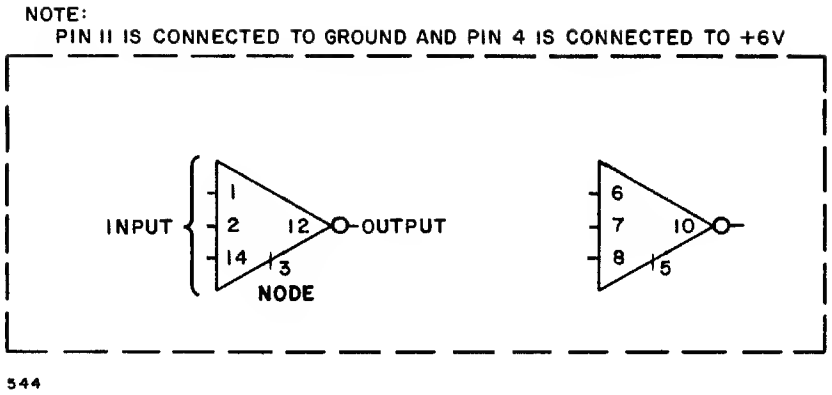


Figure A-7. Type F-03 Power Amplifier Equivalent Logic Symbol

Circuit Delay

(Measured at the +1.5v level, averaged over two stages)

24 nsec (typ)

30 nsec (max)

The maximum delay is specified with a total of 250 pf capacitance and a dc current equivalent to 25 input gates.

TYPE F-04 FLIP-FLOP CHARACTERISTICS

The standard μ-PAC integrated circuit flip-flop, type F-04, is a double-rank, J-K flip-flop with dc set and reset capability. Figure A-8 shows the logic symbol and equivalent logic circuit.

The clock gate portion of the flip-flop is composed of the clock and the set and reset control inputs. The control inputs are energized by logic ONEs. A ZERO-ONE-ZERO pulse on the clock will cause the flip-flop to assume the state determined by the condition of the control inputs. With J-K circuitry, no combination of the control input signals can cause an ambiguous state.

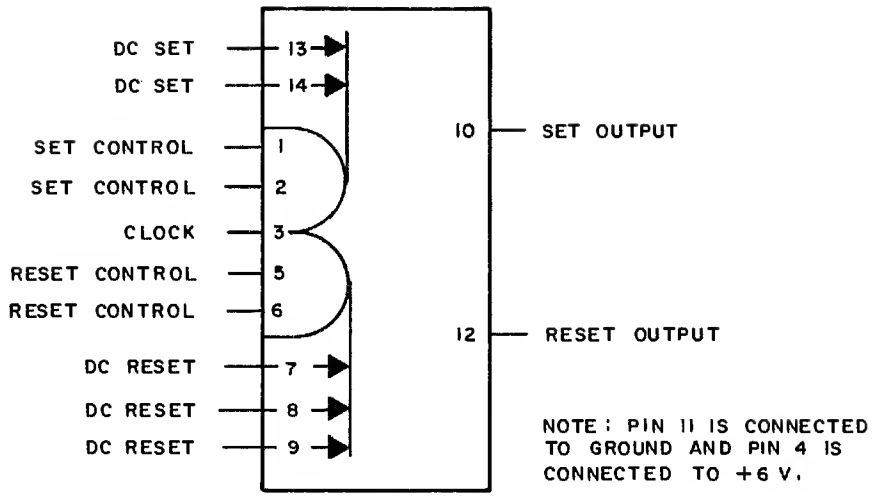
The set and reset control inputs may be used as follows.

a. To gate clock pulses

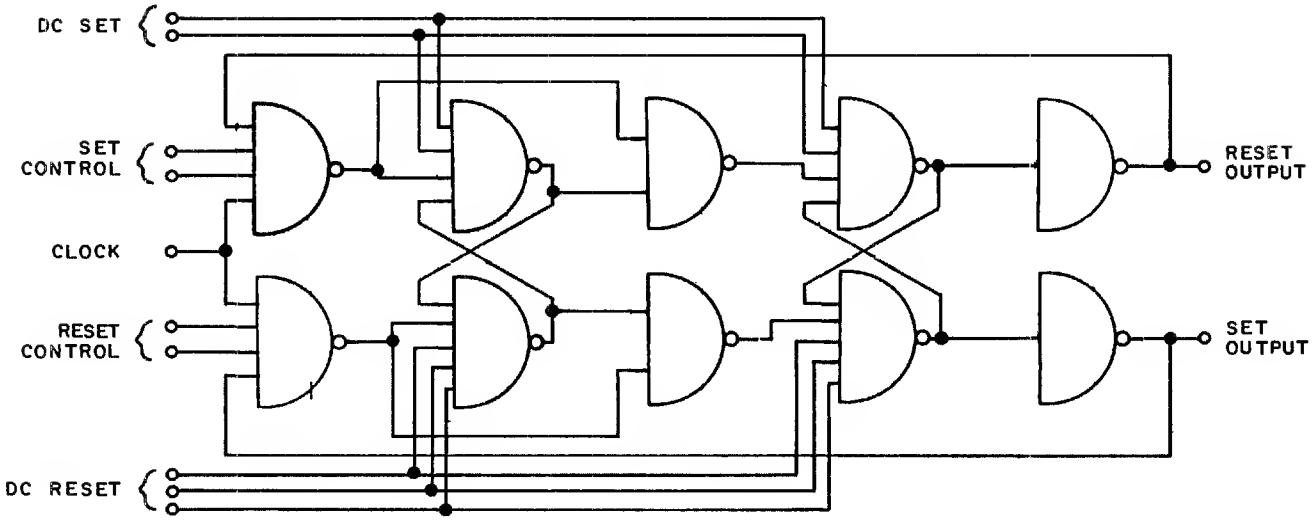
b. As direct set and reset inputs

c. As another clock input when a set and a reset control are tied together.

For dc operation, voltage levels are used on the dc inputs. Signals applied to the dc set and reset inputs take precedence over any ac gating. However, output spikes may occur when the reset clock gate is activated during a dc set, or vice-versa. Such spikes can be eliminated by tying the dc set input to a reset control input and tying the dc reset input to a set control input.



A. LOGIC SYMBOL



B. EQUIVALENT LOGIC CIRCUIT

Figure A-8. Type F-04 Flip-Flop Logic Symbol and Equivalent Logic Circuit

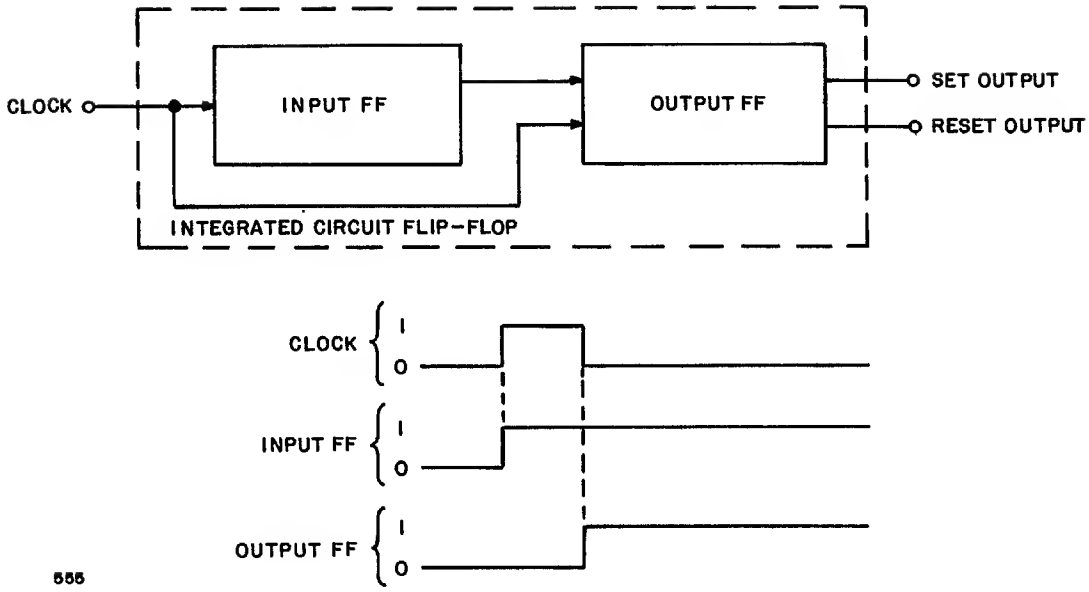


Figure A-9. Double-Rank Flip-Flop Pulse Dodging, Timing Diagram

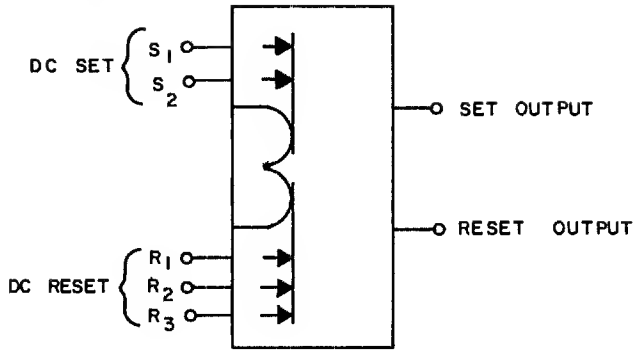
Pulse Dodging

The flip-flop utilizes the double-rank technique of pulse dodging (Figure A-9). When the clock input makes the transition from ZERO to ONE, the state of the input flip-flop is fixed and data transfer from the input flip-flop to the input of the output flip-flop is inhibited. On the ONE to ZERO transition of the clock input, data from the input flip-flop is shifted to the output flip-flop and the inputs to the input flip-flop are inhibited. Thus the clock provides intrinsic pulse dodging by means of trailing edge triggering. This feature permits strobing of the flip-flop output with input triggering signals.

DC Operation

If either dc set goes to logic ZERO, the flip-flop will assume the ONE state; if any dc reset goes to ZERO, the flip-flop will assume the ZERO state. If both a dc set and a dc reset go to ZERO at the same time, both the set and the reset outputs will go to logic ZERO. Figure A-10 contains diagrams and equations describing this mode of flip-flop operation.

A.) LOGIC DIAGRAM



B) Truth Table and Boolean Equations

S_D - AND result of the dc set inputs. $S_D = S_1 \cdot S_2$

R_D - AND result of the dc reset inputs. $R_D = R_1 \cdot R_2 \cdot R_3$

F - state of the flip-flop (set output)

F' - previous state of the flip-flop

S_D	R_D	F
0	0	(Both set and reset outputs are 0's.)
0	1	1
1	0	0
1	1	F' (no change)

$$F = R_D (\overline{S}_D + F')$$

C.) TIMING DIAGRAM

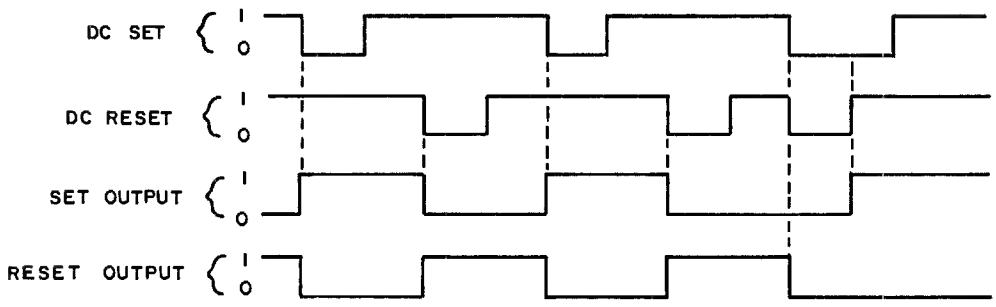


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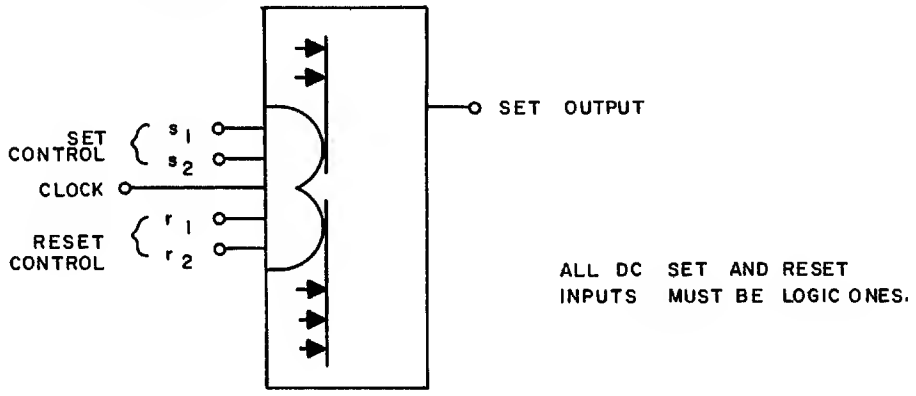
Figure A-10. DC Operation

Control Inputs Used to Steer Clock Pulses

If both the set controls (S_C) and the reset controls (R_C) are logic ONES, the flip-flop will be complemented by the application of a clock pulse. If only S_C or R_C is a ONE, the state of the flip-flop will be a ONE or ZERO, respectively, after the clock is energized. If both S_C and R_C are ZERO, the flip-flop will remain in its previous state. One restriction is that when a control input is used to gate the clock, the control input cannot change from the ONE to the ZERO state while the clock is a ONE. Figure A-11 contains diagrams and equations describing this mode of flip-flop operation.

A) LOGIC DIAGRAM



B) Truth Table and Boolean Equations

S_C - AND result of the set control inputs, $S_C = s_1 \cdot s_2$

R_C - AND result of the reset control inputs, $R_C = r_1 \cdot r_2$

F' - previous state of the flip-flop

F - state of the flip-flop after the clock pulse

S	R	F'	F	
0	0	0	0	NO CHANGE
0	0	1	1	
0	1	0	0	RESET
0	1	1	0	
1	0	0	1	SET
1	0	1	1	
1	1	0	1	COMPLEMENT
1	1	1	0	

$$F = S_C \overline{F'} + \overline{R_C} F'$$

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Figure A-11. Control Inputs Used to Gate Clock Pulses (Sheet 1 of 2)

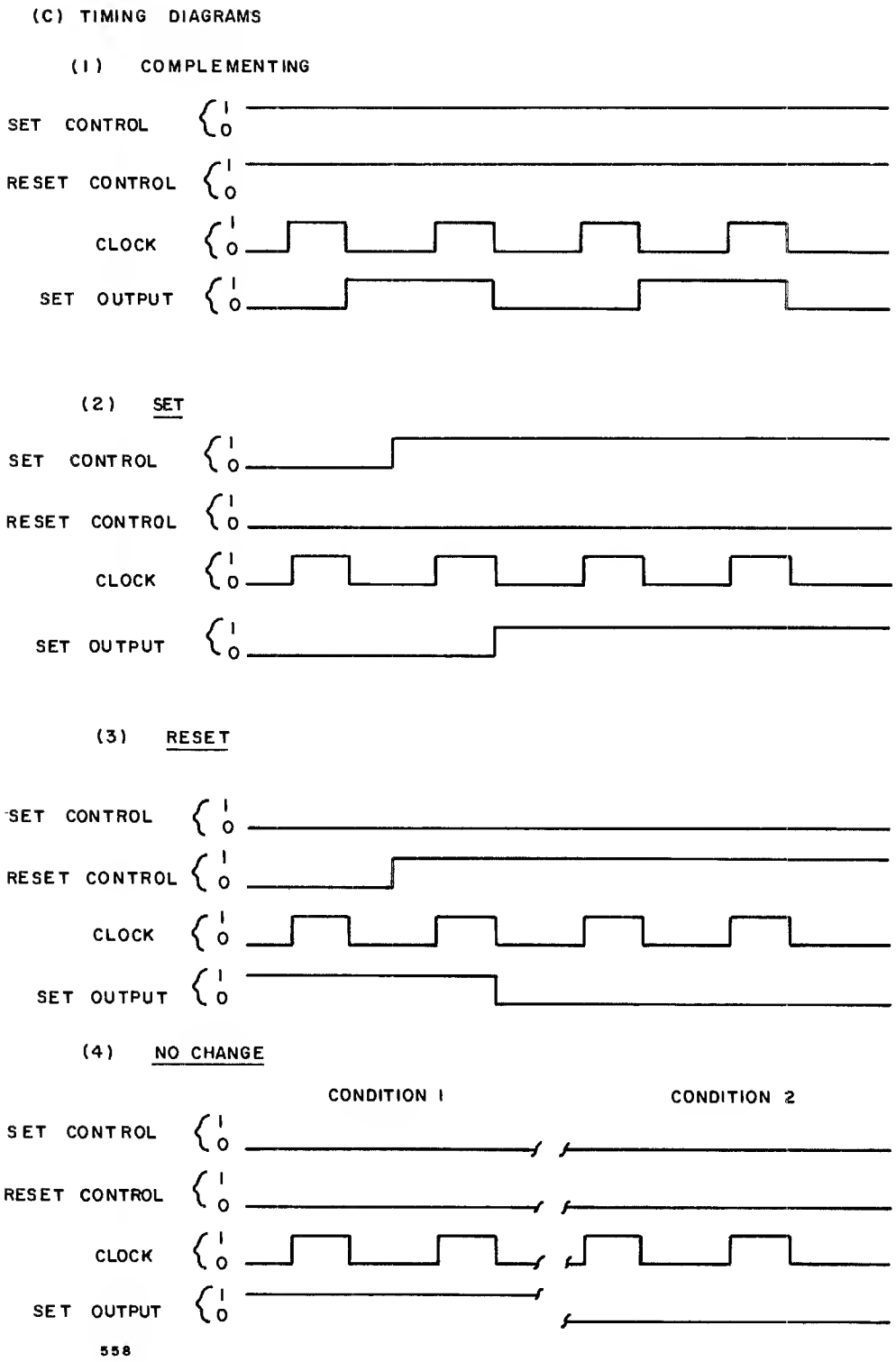


Figure A-11. Control Inputs Used to Gate Clock Pulses (Sheet 2 of 2)

Control Inputs Used as a Second Clock

A set and a reset control can be tied together and used as another clock input. In this case, the resultant clock is the ANDed result of both clocks. Figure A-12 contains diagrams describing this mode of flip-flop operation.

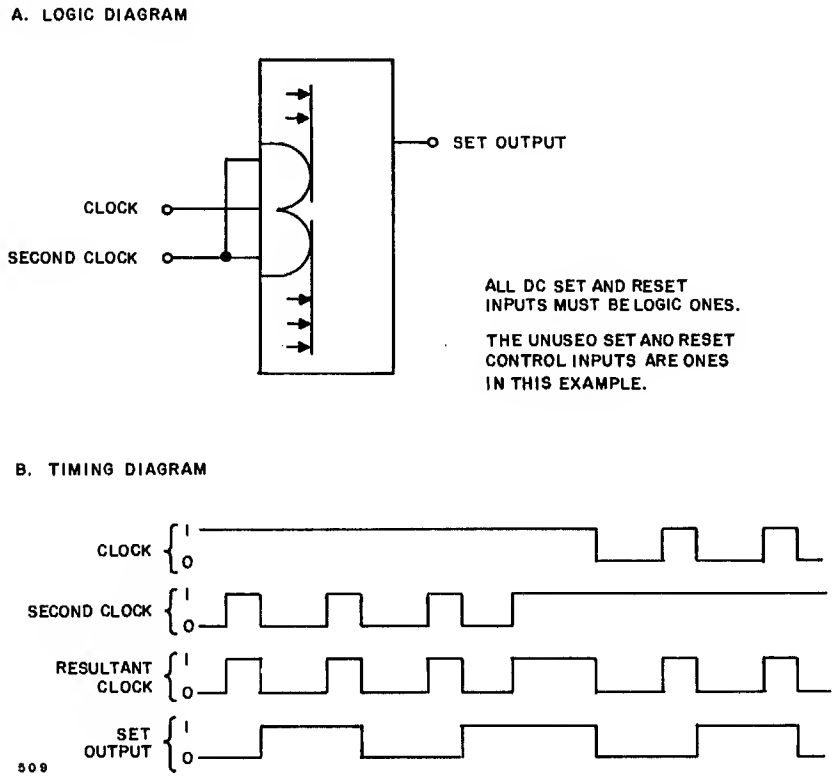
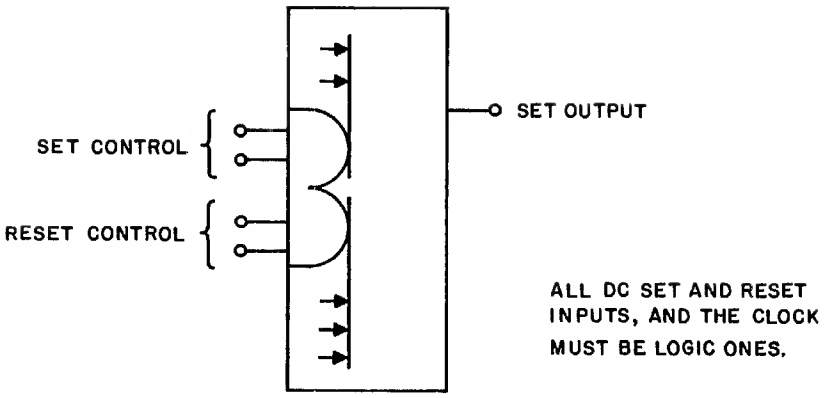


Figure A-12. Control Inputs Used As a Second Clock

Control Inputs Used Directly to Set or Reset

The set and the reset control inputs can also be used separately to change the state of the flip-flop. When the clock is a ONE, the first control input that goes from ONE to ZERO acts as the clock input. After a set control changes from ONE to ZERO, the flip-flop will be in the ONE state. After a reset control changes from ONE to ZERO, the flip-flop will be in the ZERO state. Figure A-13 contains diagrams and equations describing this mode of flip-flop operation.

A. LOGIC DIAGRAM



B) Boolean Equations

S_C - AND result of the set control inputs

R_C - AND result of the reset control inputs

F - state of the flip-flop

primes (') - previous state of a signal

$F = S'_C \cdot \overline{S}_C$ (setting operation)

$\overline{F} = R'_C \cdot \overline{R}_C$ (resetting operation)

C. TIMING DIAGRAM

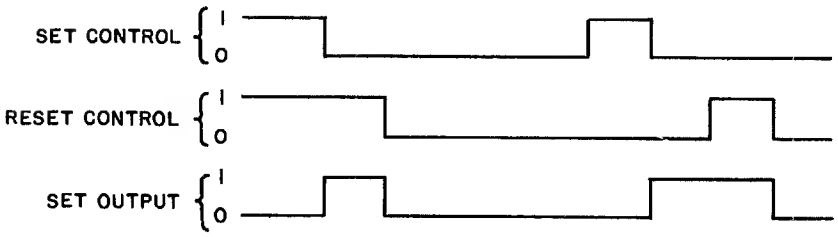


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Figure A-13. Control Inputs Used Directly to Set or Reset

Input Loading

DC inputs:	2/3 unit load
Clock input:	1 unit load
Control inputs:	1 unit load

Output Drive Capability

8 unit loads (both outputs)
(Capable of also driving 75 pf total capacitance with delays as specified.)

Circuit Delay

The following circuit delays are specified from the +1.5v level of the input signal to the +1.5v level of the output signal.

Clock input (ONE to ZERO transition) to latest output	45 nsec (typ) 60 nsec (max)
DC set input to set output or DC reset input to reset output	65 nsec (typ) 80 nsec (max)
DC set input to reset output or DC reset input to set output	45 nsec (typ) 60 nsec (max)

Clock and Control Input Timing Requirements

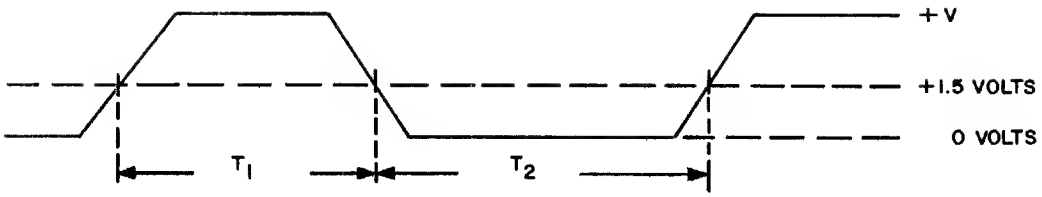
To trigger the flip-flop at the clock or control inputs, pulses must meet the requirements shown in Figure A-14.

DC Input Timing Requirements

To activate a dc input, signals must meet the requirements of Figure A-15.

Control Inputs

Figure A-16 shows the timing requirements of the set and reset control inputs when they are being used to steer the triggering clock input to set the flip-flop. The reset control input must be completely switched to logic ZERO before the clock starts positive. No control input should go from logic ONE to ZERO while the clock is positive. The set control input must be switched to logic ONE at least 40 nsec before the clock starts towards logic ZERO. The clock must be a positive pulse of 40 nsec minimum duration. The flip-flop changes state on the trailing edge of the positive clock pulse. Reset timing is the same, except that the time relations and logic levels of the set and reset input must be interchanged.



T_1 (POSITIVE TIME) = 40 NSEC. (MIN)

T_2 (NEGATIVE TIME) = 60 NSEC. (MIN)

+V (INPUT ONE LEVEL) = +3.0 VOLTS (MIN)

T_{RISE} AND T_{FALL} REQUIREMENT – ANY μ-PAC OUTPUT SIGNAL WILL RELIABLY TRIGGER THE FLIP-FLOP.

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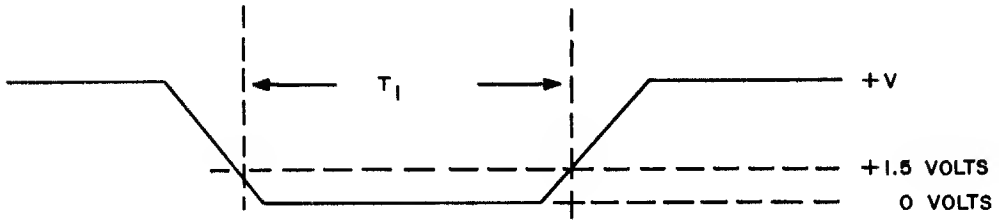
Figure A-14. Flip-Flop Input Pulse Requirements



T_1 (TIME AT LOGIC ZERO) = 80 NSEC. (MIN.)

V (INPUT ONE LEVEL) = +3.0 VOLTS (MIN.)

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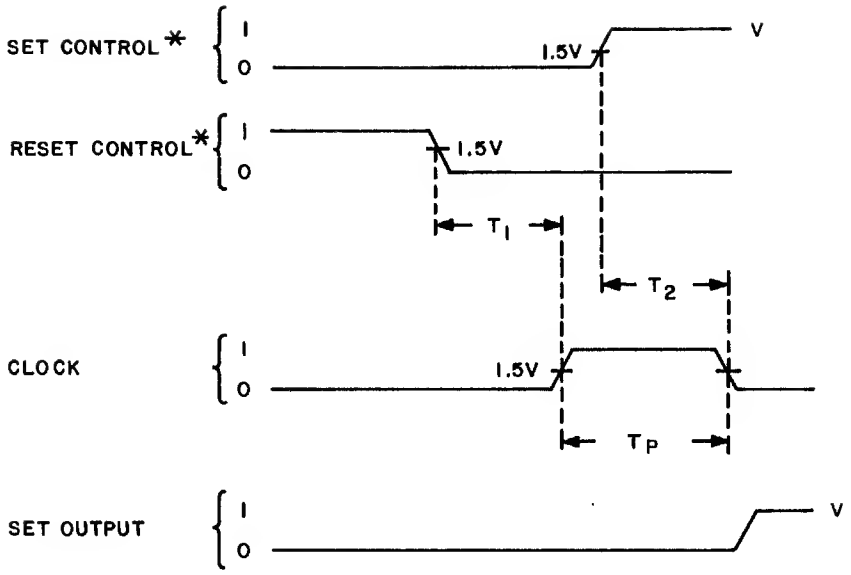
Figure A-15. DC Set and Reset Input Signal Requirements

Maximum Allowable Clock Skew

In cases where a register is being driven by clock (shift) signals from different sources, the output of one stage may arrive at the next stage before late clock signal. If the delay between the early and late clock signals is more than 30 nsec, erroneous data transfer may occur. To guarantee proper operation the allowable clock skew must be as shown in Figure A-17. Note that the triggering signal to flip-flop B is S_A rather than C_B. This situation is not detrimental to the operation of the shift register. Either S_A or C_B may trigger flip-flop B, depending on which occurs first.



*INTERCHANGE SET AND RESET CONTROL TIMING TO RESET THE FLIP-FLOP

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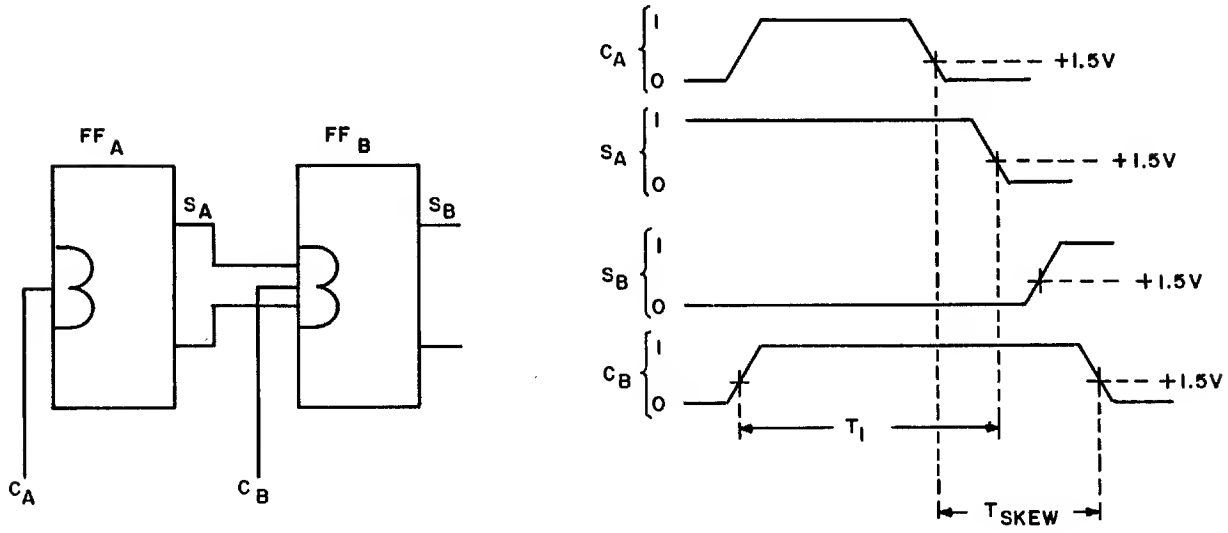
(T_1) = 0 (MIN)

(T_2) = 40 NSEC (MIN)

(T_P) = 40 NSEC (MIN)

(V) = 3.0 VOLTS (MIN)

Figure A-16. Timing Requirements for Control Inputs, Using Clock Triggering



$T_{SKEW} \leq$ 30 NANOSEC.

A563 $T_1 \geq$ 40 NANOSEC.

Figure A-17. Allowable Clock Skew, Logic and Timing

TYPE F-09 POWER AMPLIFIER CHARACTERISTICS

The type F-09 power amplifier microcircuit has two 4-input inverter amplifiers with nodes for input gating expansion. (See Figure A-18.) The power amplifier circuit is logically equivalent to the NAND gate but has about three times the output drive capability. It has a short circuit protection network such that accidental grounding of the output will not damage the circuit.

Input Loading

2 unit loads

Output Drive Capability

25 unit loads (capable of also driving 250 pf total capacitance with delays as specified)

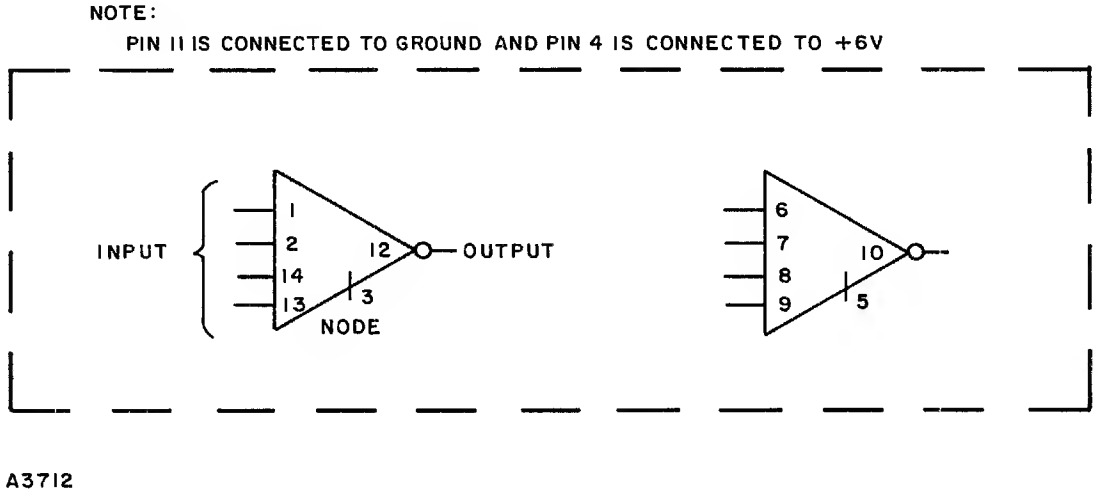


Figure A-18. Type F-09 Power Amplifier Equivalent Logic Symbol

Circuit Delay

(Measured at 1.5v level, averaged over two stages)

30 nsec (max) - 25 unit loads plus 250 pf stray capacitance

15 nsec (max) - 12 unit loads plus 70 pf stray capacitance

Unless specified otherwise, the general μ-PAC characteristics also apply to the type F-09 microcircuit.

DRIVER MATRIX PAC, MODEL CC-002

GENERAL DESCRIPTION

The Driver Matrix PAC, Model CC-002, contains a three-by-six diode-resistor selection matrix and three transistor lamp driver circuits. Each lamp driver is capable of switching up to 40 ma of current from a positive supply of up to 28v. The CC-002 operates from standard μ-PAC logic levels.

CIRCUIT FUNCTION

The selection matrix has six control lines, each of which controls three inputs (Figure A-19). A positive supply (+6v) applied to a control line enables the three inputs associated with it; a ground (0v) will inhibit them.

During normal operation, only one control line is enabled, the others being held at 0v. When one of the inputs controlled by the enabled line is passive, the transistor in that circuit is saturated and the lamp turns on. When the input is active, the transistor is biased off and the lamp is extinguished.

A resistor is connected across each of the lamp driver outputs to maintain a small lamp current during its OFF state. This prevents high transient currents from occurring when the lamp is illuminated.

SPECIFICATIONS

Frequency of Operation

DC to 200 kc

Input Loading

1 unit load

Power Dissipation

0.1w (max, if only one control line is enabled)

Output Drive Capability

40 ma at +28v

Current Requirements

+6v: 5 ma (max, if only one control line is enabled)

NOTE

This document contains the information stated in Revision A of 3C Document No. A008678.

Electrical Parts List

Ref. Desig.	Description	3C Part No.
CR1-CR13	DIODE: Replacement Type 1N914	943 083 001
R1-R6	RES, fxd, film: 3.3K ±2%, 1/4w	932 114 061
R7	RES, fxd, film: 2.2K ±2%, 1/4w	932 114 057
R8	RES, fxd, comp: 2.26K ±3%, 1/2w	932 209 218
Q1	TSTR	943 744 003

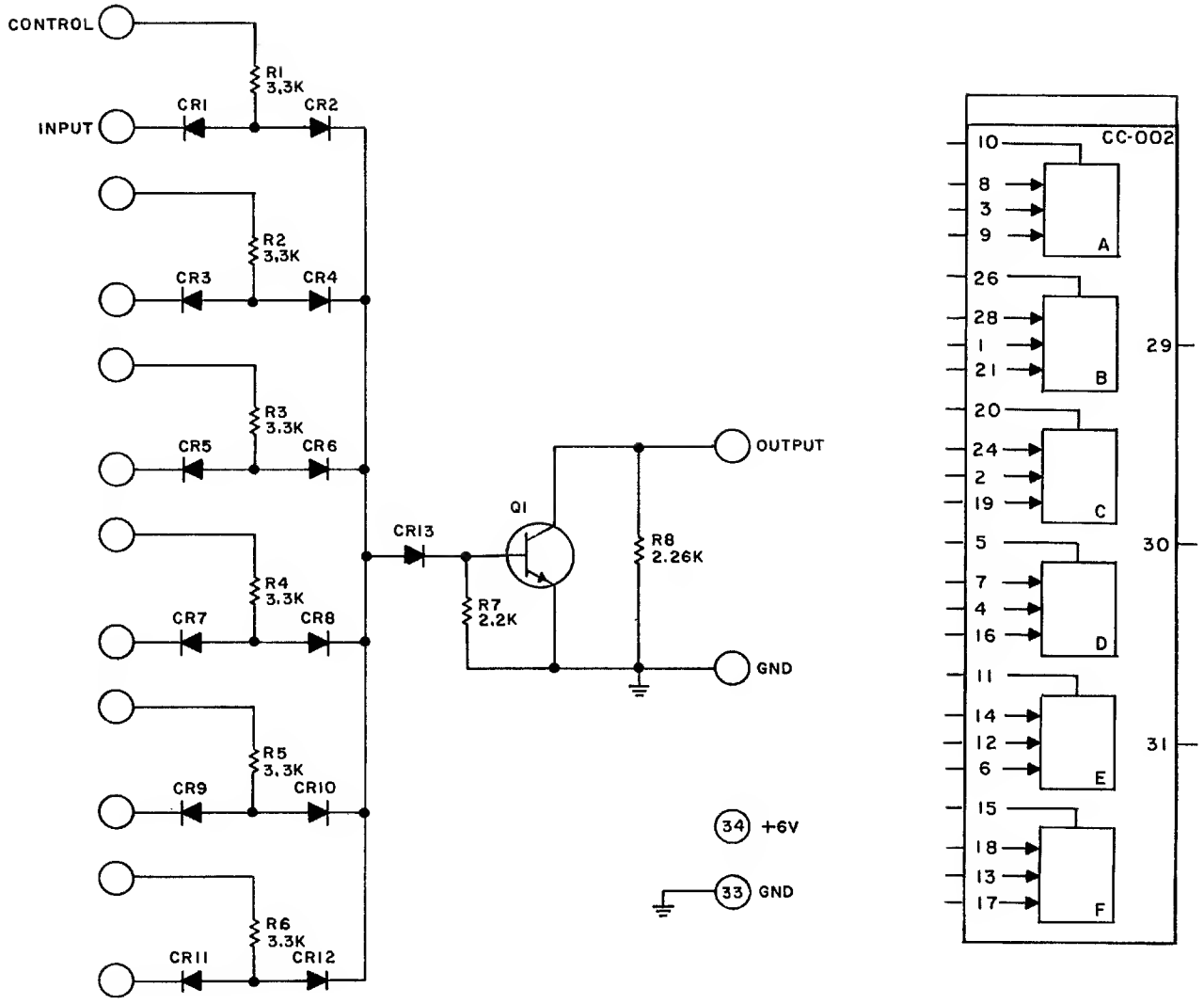


Figure A-19. Driver Matrix PAC, Model CC-002, Schematic Diagram and Logic Symbol

CARRY MOST SIGNIFICANT BIT PAC, MODEL CC-034

GENERAL DESCRIPTION

The Carry Most Significant Bit PAC, Model CC-034 (Figure A-20), contains four F-01 microcircuit gates and three F-09 microcircuit amplifiers. These circuits are interconnected to form the most significant bits of the carry net of a digital computer.

SPECIFICATIONS

Frequency of Operation

DC to 5 MHz

Input Loading

1 unit load per F-01 gate
2 unit loads per F-09 amplifier

Circuit Delay (measured at 1.5v, averaged over two stages)

F-01 gates:	30 ns (max)
F-09 amplifiers:	15 ns (max) with 70 pf stray capacitance and 12 unit loads

Output Drive Capability

Pins	Unit Loads Each
8, 10, 18, 20	12
6	8
22	7
4	4
26	3
17	8

Current Requirements

+6v: 111 ma (max)

Power Dissipation

0.67w (max)

Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1-M3	MICROCIRCUIT: F-09 power amplifier integrated circuit	950 100 009
M4-M7	MICROCIRCUIT: F-01 dual NAND gate integrated circuit	950 100 001
C1, C2	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 µf ±20%, 50 vdc	930 313 016
CR1-CR14	DIODE: Replacement Type IN914	943 083 001

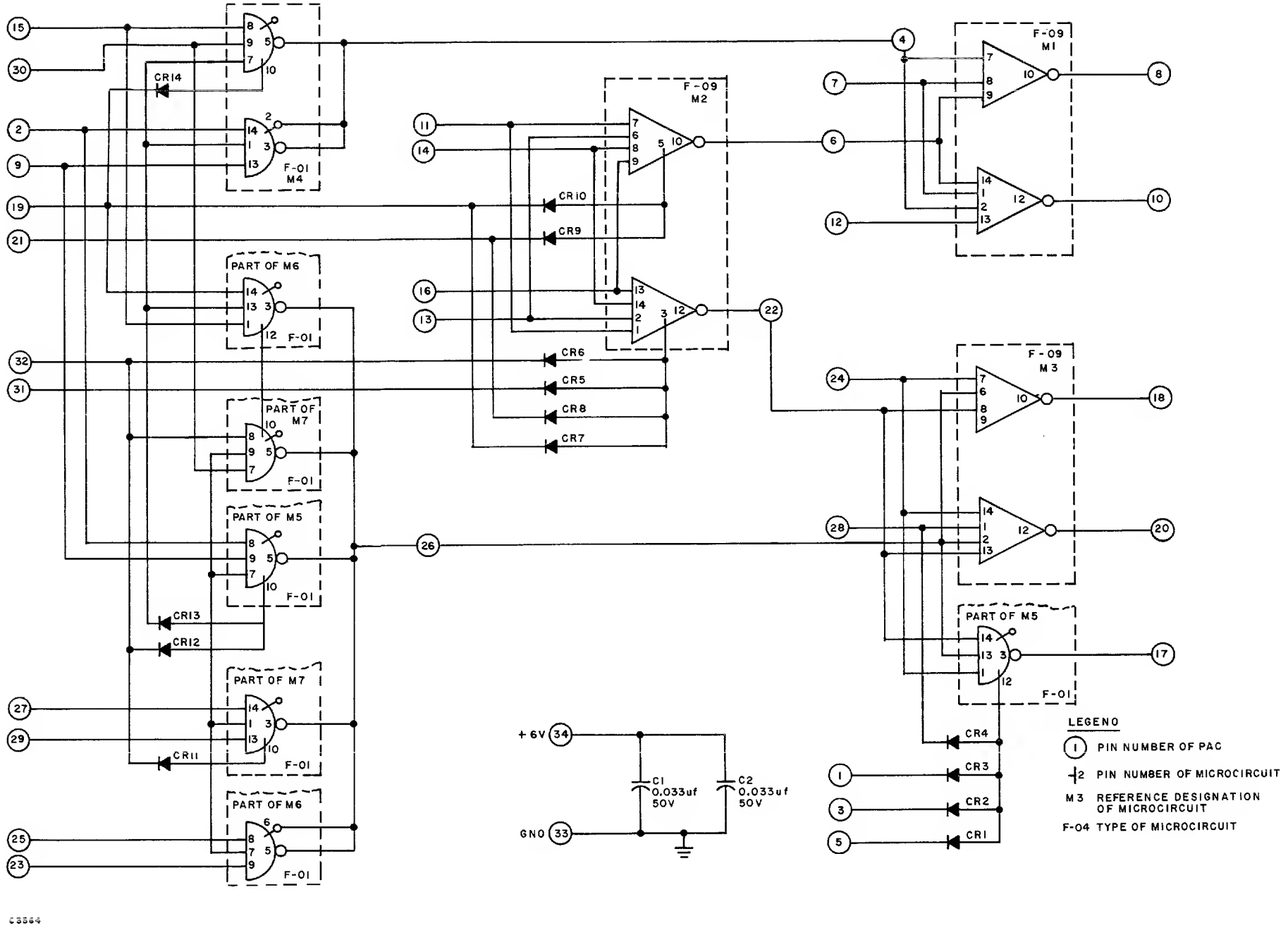


Figure A-20. Most Significant Bit PAC, Model CC-034, Schematic Diagram

CARRY MIDDLE BITS, MODEL CC-035

GENERAL DESCRIPTION

The Carry Middle Bits PAC, Model CC-035 (Figure A-21), contains two F-01 microcircuit gates and five F-09 microcircuit amplifiers. These circuits are interconnected to form the middle bits of the carry net of a digital computer.

SPECIFICATIONS

Frequency of Operation

DC to 5 MHz

Input Loading

1 unit load per F-01 gate
2 unit loads per F-09 amplifier

Output Drive Capability

Pins	Unit Loads Each
8, 11, 13, 23, 25, 26, 28	12
10	10
22, 27	8
21	4

Circuit Delay (measured at +1.5v, averaged over two stages)

F-01 gates	30 ns (max)
F-09 amplifiers	15.0 ns (max) with 70 pf of stray capacity and 12 unit loads

Current Requirements

+6v: 143 ma (max)

Power Dissipation

0.86w (max)

Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1-M3, M6, M7	MICROCIRCUIT: F-09, power amplifier integrated circuit	950 100 009
M4, M5	MICROCIRCUIT: F-01, NAND gate integrated circuit	950 100 001
C1, C2	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
CR1-CR3	DIODE	943 083 001

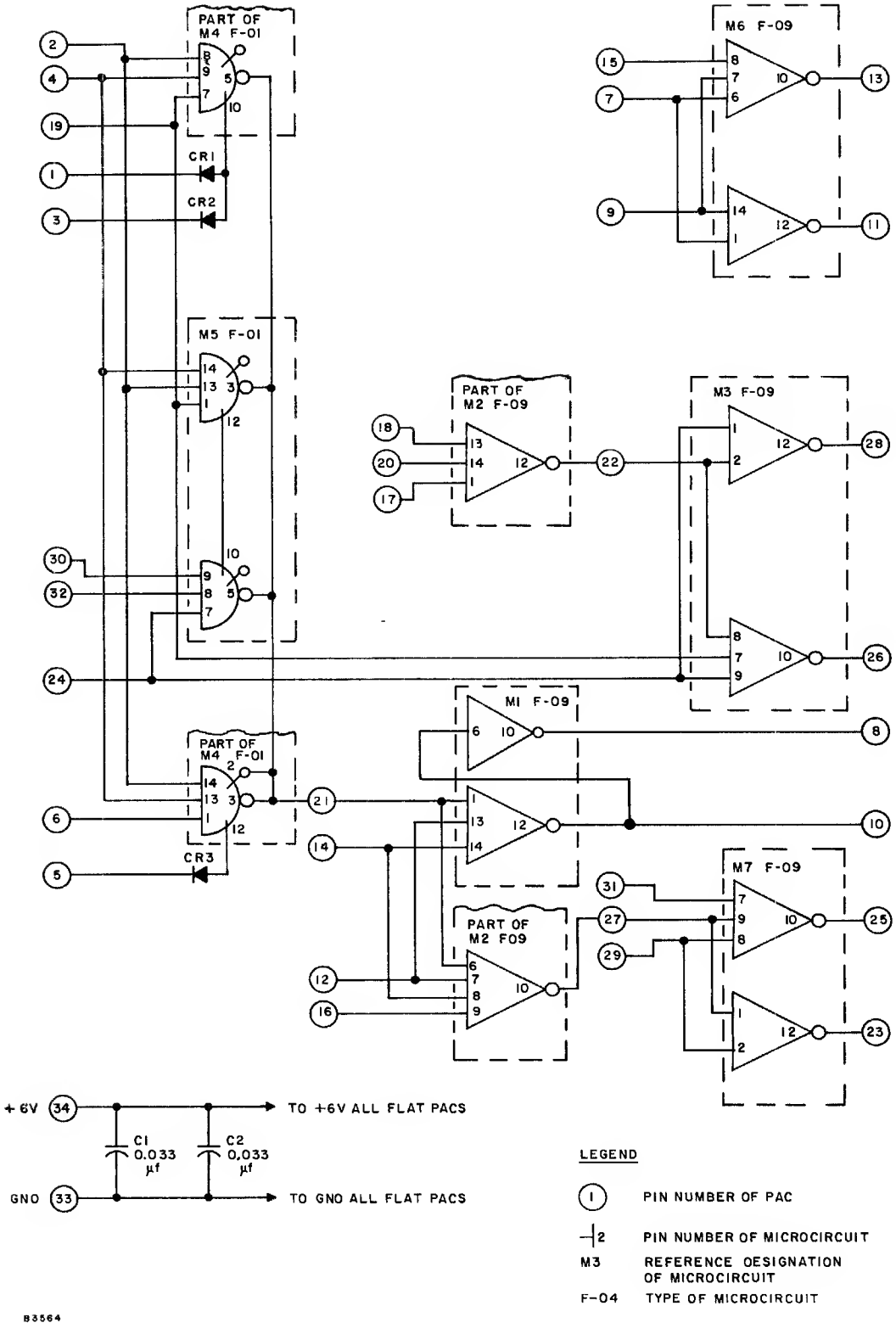


Figure A-21. Carry Middle Bits PAC, Model CC-035, Schematic Diagram

CARRY LEAST SIGNIFICANT BIT PAC, MODEL CC-036

GENERAL DESCRIPTION

The Carry Least Significant Bit PAC, Model CC-036 (Figure A-22), contains one F-01 microcircuit gate and six F-09 microcircuit amplifiers. These circuits are interconnected to form the least significant bits of the carry net of a digital computer.

SPECIFICATIONS

Frequency of Operation

DC to 5 MHz

Input Loading

1 unit load per F-01 gate
2 unit loads per F-09 amplifier

Output Drive Capability

Pins	Unit Loads Each
1, 7, 31	12
32	11
30	10
24	9
20, 22	8

Circuit Delay (measured at +1.5v, averaged over two stages)

F-01 gates 30 ns (max)
F-09 amplifiers 15.0 ns (max) with 70 pf stray capacity and 12 unit loads

Current Requirements

+6v: 128 ma (max)

Power Dissipation

0.77w (max)

Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1, M2, M4-M7	MICROCIRCUIT: F-09 power amplifier integrated circuit	950 100 009
M3	MICROCIRCUIT: F-01 NAND gate integrated circuit	950 100 001
C1, C2	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 µf ±20%, 50 vdc	930 313 016
CR1-CR19	DIODE	943 083 001

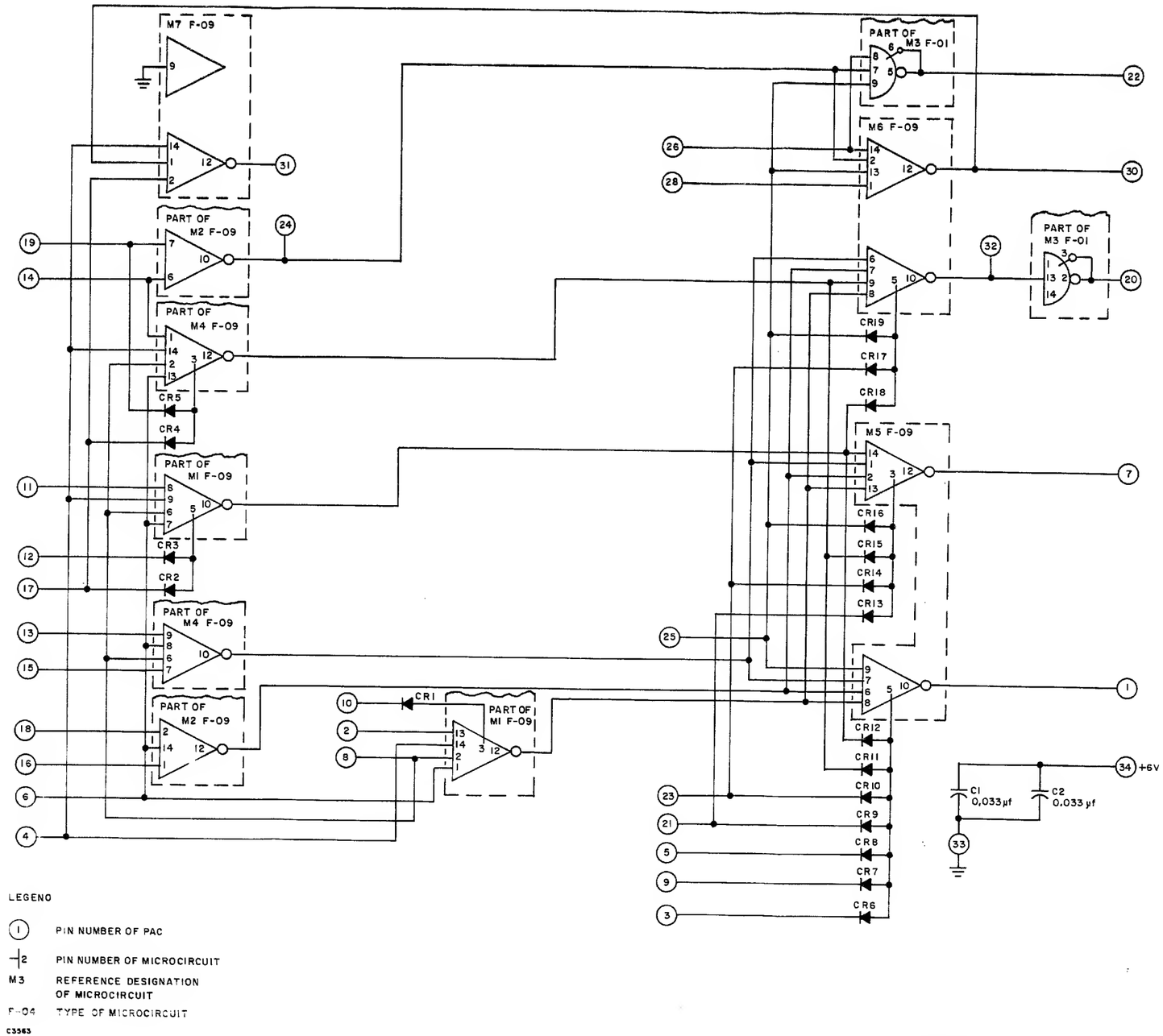


Figure A-22. Carry Least Significant Bit PAC, Model CC-036, Schematic Diagram

COLUMN BEX PAC, MODEL CC-037

GENERAL DESCRIPTION

The Column BEX PAC, Model CC-037 (Figure A-23), contains six F-01 microcircuit gates and four F-02 microcircuit gates. These gates are interconnected to form two bits of each of the following:

B Register - Extended Accumulator
E Register
X Register - Index Register

SPECIFICATIONS

Frequency of Operation

DC to 5 MHz

Input Loading

1 unit load per F-01 gate
1 unit load per F-02 gate

Output Drive Capability

Pins	Unit Loads Each
7, 12, 16, 18	8
11, 15	7
3, 22	5
10, 14, 27, 29	2

Circuit Delay (measured at +1.5v, averaged over two stages)

30 ns (max)

Current Requirements

162 ma (max)

Power Dissipation

0.97w (max)

Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1, M2, M4, M6, M9, M10	MICROCIRCUIT: F-01, dual NAND gate integrated circuit	950 100 001
M3, M5, M7, M8	MICROCIRCUIT: F-02, quad NAND gate integrated circuit	950 100 002
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 µf ±20%, 50 vdc	930 313 016

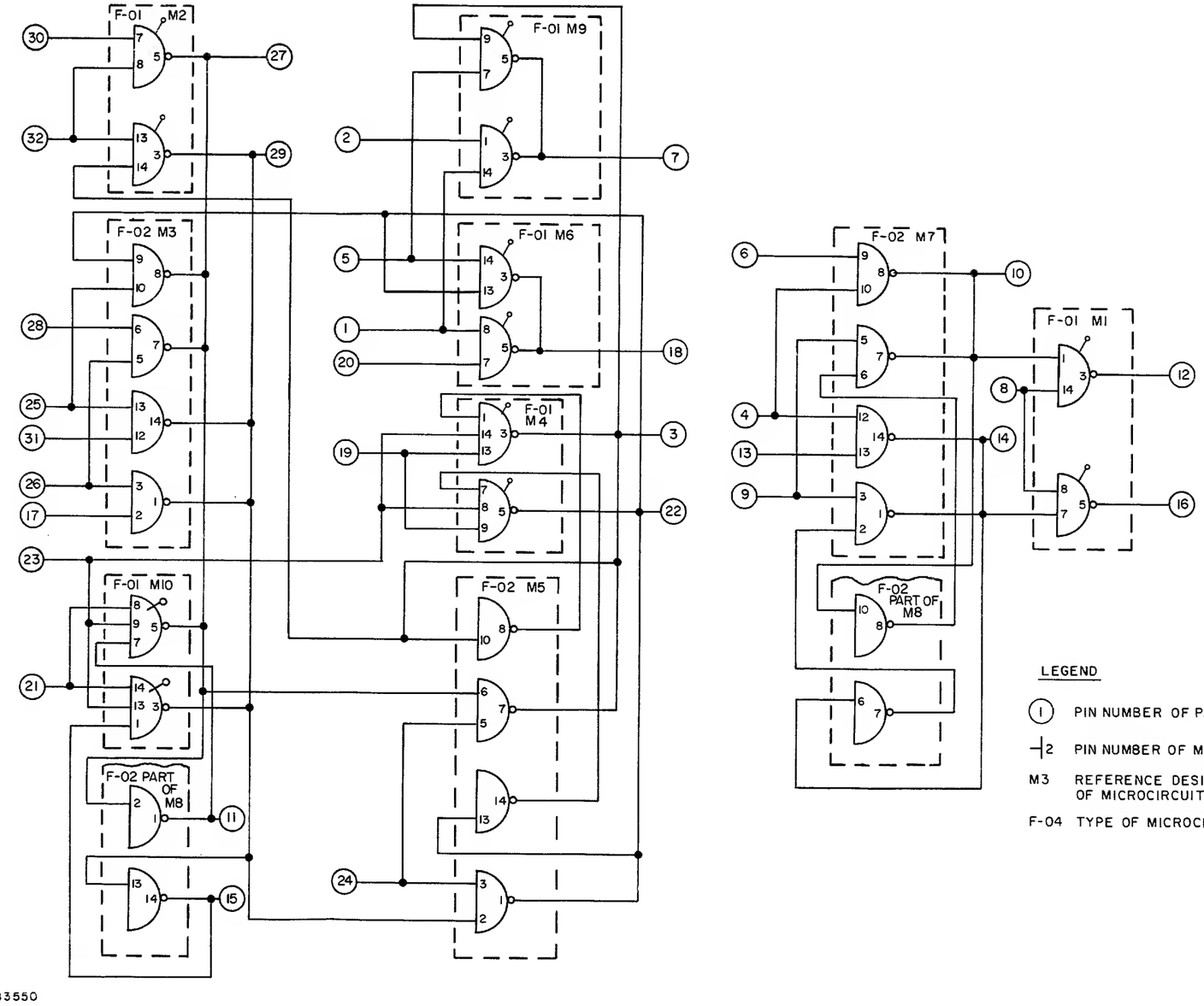


Figure A-23. Column BEX PAC, Model CC-037, Schematic Diagram

COLUMN DISTRIBUTION REGISTER AND MEMORY INFORMATION REGISTER BIT PAC, MODEL CC-038

GENERAL DESCRIPTION

The Column Distribution Register and Memory Information Register Bit PAC, Model CC-038 (Figure A-24), is a functional module containing one F-02, three F-09 and three F-01 flat placks. Three diode clusters are provided for node expansion on the F-01 gates. An input bus termination resistor and diode are provided at the input to pin 5 to pull the input signal to +6 volts. Functionally, the PAC provides one bit of Distribution Register and one bit of the Memory Information Register of the computer.

SPECIFICATIONS

Frequency of Operation

DC to 5 MHz

Input Loading

F-01 and F-02 inputs:
1 unit load

F-09 inputs: 2 unit loads

Output Drive Capability

Pin	μ-Loads
28	2
29, 17	6
32	12 (25 as F-03)
11	6
16, 26	11
23, 25	9
6	7

Circuit Delay (measured at +1.5v, averaged over two stages)

F-01: 30 ns (max)
F-02: 30 ns (max)
F-09: 15 ns (max) with 12 unit loads and 70 pf stray capacitance

Current Requirements

+6v: 120 ma (max)

Power Dissipation

720 mw (max)

Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1, M2, M6	MICROCIRCUIT: F-09, power amplifier integrated circuit	950 100 009
M3, M4, M7	MICROCIRCUIT: F-01, dual NAND gate integrated circuit	950 100 001
M5	MICROCIRCUIT: F-02, quad NAND gate integrated circuit	950 100 002
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
CR1-CR9	DIODE: Replacement Type IN914	943 083 001
R1	RESISTOR, FIXED, COMPOSITION: 510 ohms ±5%, 1/4w	932 007 042

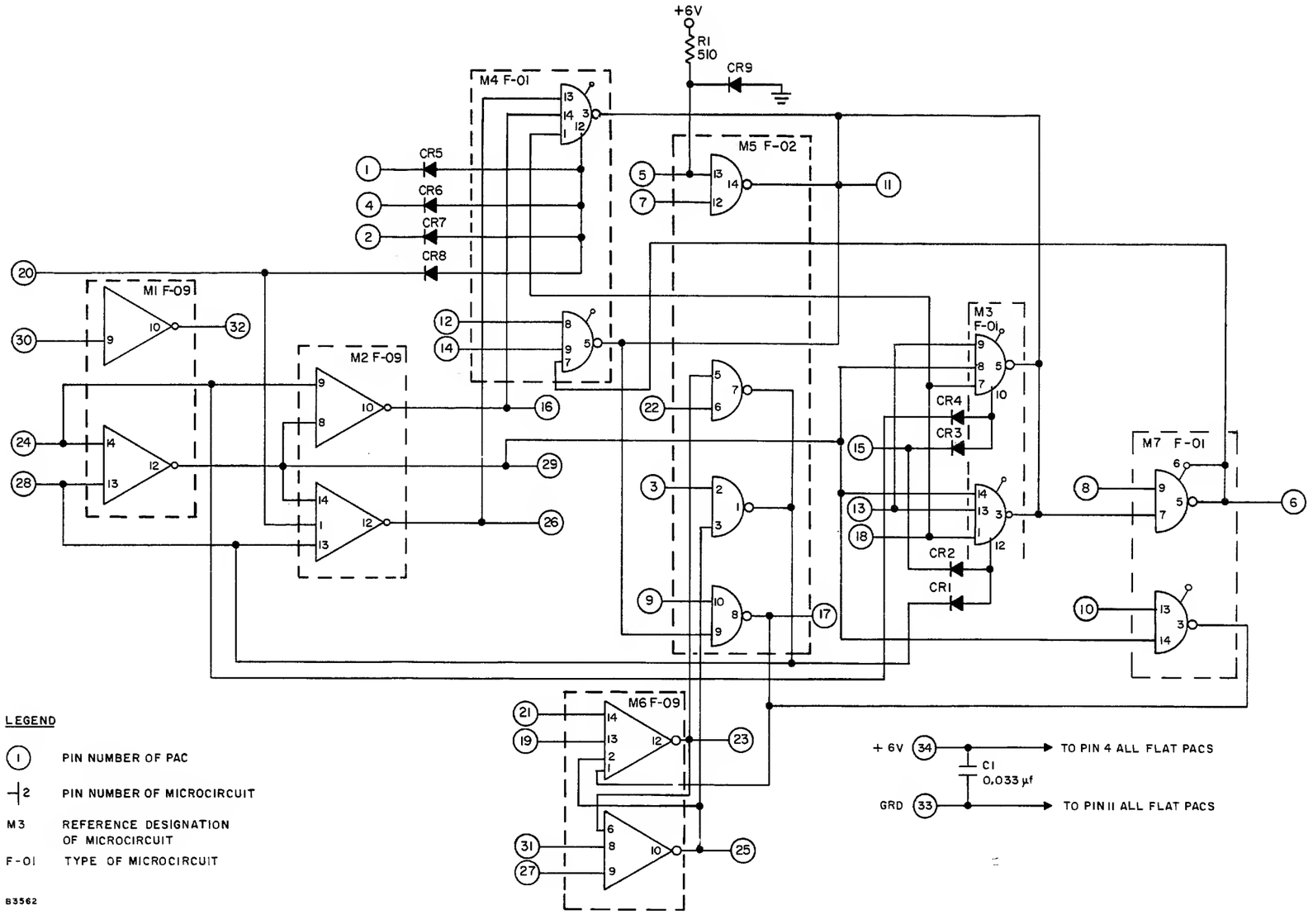


Figure A-24. Column Distribution Register and Memory Information Register Bit PAC Model CC-038

COLUMN PAY PAC, MODEL CC-039

GENERAL DESCRIPTION

The Column PAY PAC, Model CC-039 (Figure A-25), is a functional module which contains seven F-01, three F-02 and one F-09 flat packs plus one discrete diode utilized for input expansion of an F-01 gate. Functionally it provides two bits each of the Program Counter, Accumulator and the Memory Address Register of a computer.

SPECIFICATIONS

Frequency of Operation

DC to 5 MHz

Input Loading

F-01, F-02 inputs - 1 unit load each

Output Drive Capability

Pins	μ-Loads
5, 25	1
6, 8, 10, 16	7
9, 19	8
13, 27	6
30, 32	11

Circuit Delay (measured at +1.5v, averaged over two stages)

F-01: 30 ns (max)
F-02: 30 ns (max)
F-09: 15 ns (max) with 12 unit loads and 70 pf stray capacitance

Current Requirements

+6v: 158 ma (max)

Power Dissipation

950 mw (max)

Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1	MICROCIRCUIT: F-09, power amplifier integrated circuit	950 100 009
M2-M4, M6-M8, M10	MICROCIRCUIT: F-01, NAND gate integrated circuit	950 100 001
M5, M9, M11	MICROCIRCUIT: F-02, NAND gate integrated circuit	950 100 002
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
CR1	DIODE	943 083 001

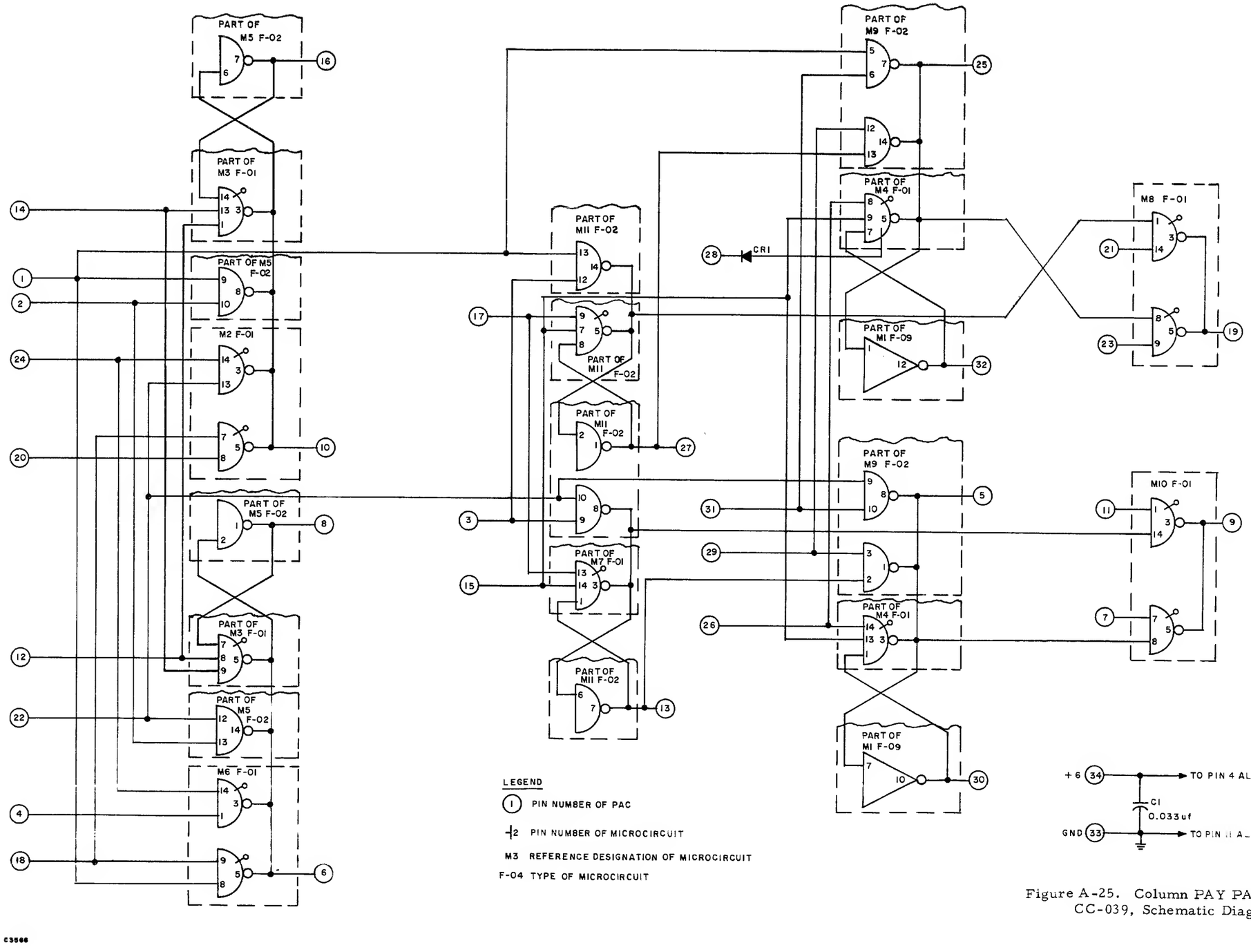


Figure A-25. Column PAY PAC, Model CC-039, Schematic Diagram

POWER FAILURE SENSE PAC, MODEL CC-043

GENERAL DESCRIPTION

The Power Failure Sense PAC, Model CC-043 (Figure A-26), contains a circuit which monitors the ac line voltage in a system and provides an output when the input voltage drops below a predetermined level. In addition, there are sixteen 510-ohm resistors connected between the supply voltage and separate output pins.

The sensing circuit must be adjusted prior to being used in a system. The exact adjustment depends on the nominal ac line voltage and the sensitivity that the user desires. It has a range from 80 to 130v rms. The initial adjustment procedure is as follows:

1. Choose an rms voltage below that which is to be considered a power failure.
2. Using a Variac or equivalent, set the input voltage to the primary of a transformer (3C Part No. 938016001, or equivalent) at the voltage chosen in 1. Connect the secondary of the transformer to pins 1 and 3 of the CC-043, with the center tap to pin 5.
3. Adjust R7 until negative pulses just begin to appear at pin 2.

Operating in a system with nominal line voltage and with the PAC adjusted as above, pin 8 is active, while pins 4 and 12 are passive. Within 8 ms after the input voltage drops below the adjusted value, these outputs will reverse (i.e., 8 passive, 4 and 12 active) and remain. After the input voltage returns to nominal value the PAC may be reset by momentarily grounding pin 6. A clamp diode to +6v is provided at pin 12 so that a relay may be driven with this output.

SPECIFICATIONS

Input Loading

Pin 10: 1 unit load
Pin 6: 2 unit loads

Output Drive Capability

Pin 8: 6 unit loads
Pin 4: 7 unit loads
Pin 12: 8 unit loads

Frequency of Operation

50 or 60 cps input

Current Requirements

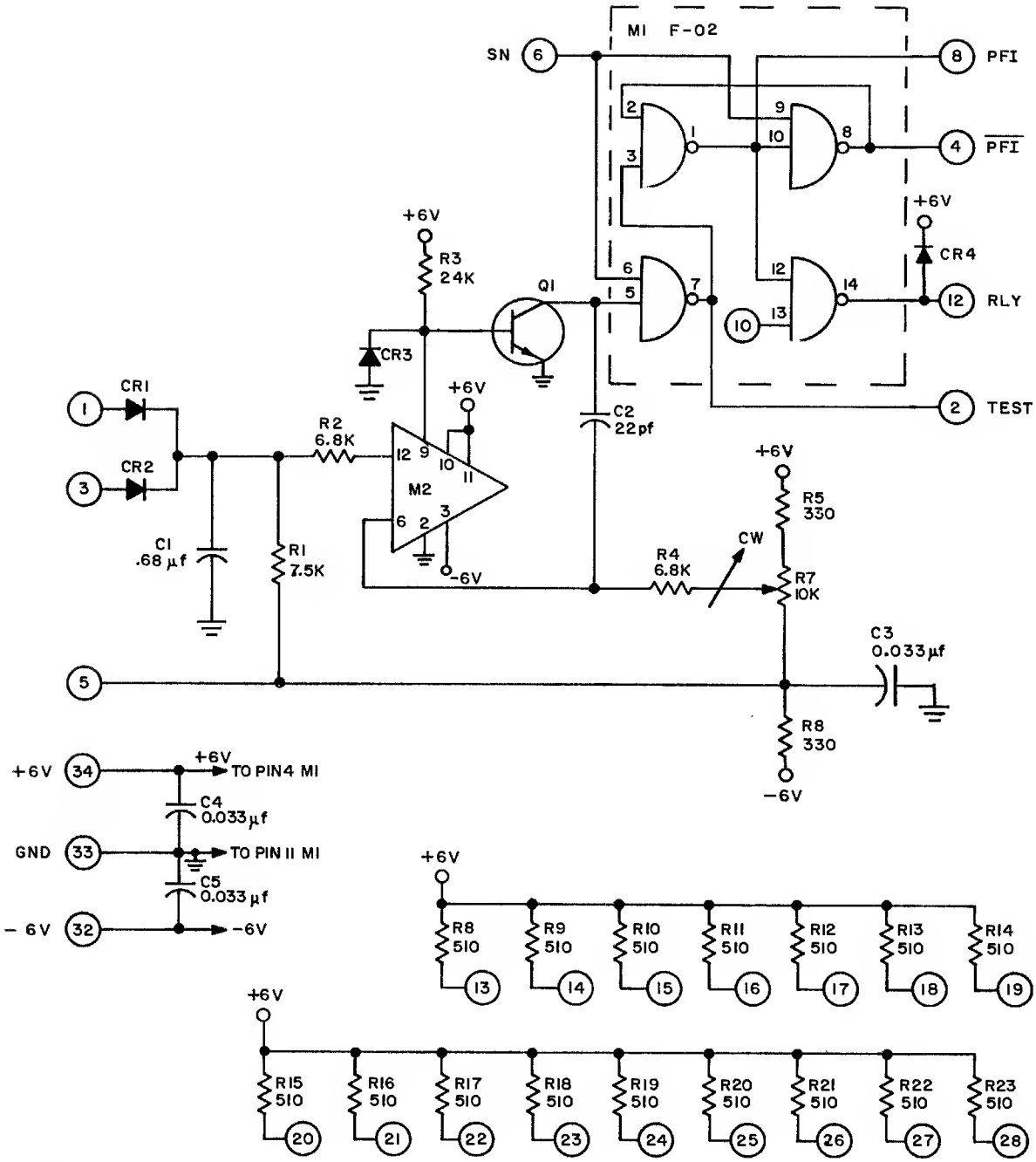
+6v: 45 ma
-6v: 10 ma

Power Dissipation

0.33w

Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1	MICROCIRCUIT: F-02, NAND gate integrated circuit	950 100 002
M2	MICROCIRCUIT: Linear amplifier integrated circuit	950 102 001
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.68 µf ±5%, 50 vdc	930 316 035
C2	CAPACITOR, FIXED, MICA DIELECTRIC: 22 pf ±5%, 100 vdc	930 004 103
C3-C5	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 µf ±20%, 50 vdc	930 313 016
CR1-CR4	DIODE	943 083 001
Q1	TRANSISTOR: Replacement Type 2N3011	943 722 002
R1	RESISTOR, FIXED, WIREWOUND: 7.5 K ±5%, 3w	932 206 133
R2, R4	RESISTOR, FIXED, FILM: 6.8 K ±2%, 1/4w	932 114 069
R3	RESISTOR, FIXED, COMPOSITION: 24 K ±5%, 1/4w	932 007 082
R5, R6	RESISTOR, FIXED, COMPOSITION: 330 ohms ±5%, 1/4w	932 007 037
R7	RESISTOR, VARIABLE, FILM: 10 K ±10%, 3/4w	933 300 107
R8-R23	RESISTOR, FIXED, COMPOSITION: 510 ohms ±5%, 1/4w	932 007 042



LEGEND

(1) PIN NUMBER OF PAC

—|2 PIN NUMBER OF MICROCIRCUIT

M3 REFERENCE DESIGNATION OF MICROCIRCUIT

F-04 TYPE OF MICROCIRCUIT

B3555

Figure A-26. Power Failure Sense PAC, Model CC-043, Schematic Diagram

PRIORITY PAC, MODEL CC-044

GENERAL DESCRIPTION

The Priority PAC, Model CC-044 (Figure A-27), contains five F-01, two F-02, and two F-03 microcircuits. They are interconnected to perform the priority function in a digital computer.

SPECIFICATIONS

Frequency of Operation

DC to 5 MHz

Input Loading

1 unit load per F-01 gate
1 unit load per F-02 gate
2 unit loads per F-03 amplifier

Output Drive Capability

Pins	Unit Loads Each
19,21,29,31	25
8,17,18,24, 28	8
6	7
11,13,23,30	4

Circuit Delay (measured at +1.5v, averaged over two stages):

30 ns (max)

Current Requirements

+6v: 160 ma (max)

Power Dissipation

0.96w (max)

Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1, M5, M7-M9	MICROCIRCUIT: F-01, dual NAND gate integrated circuit	950 100 001
M2, M6	MICROCIRCUIT: F-02, quad NAND gate integrated circuit	950 100 002
M3, M4	MICROCIRCUIT: F-03, power amplifier integrated circuit	950 100 003
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
CR1-CR19	DIODE	943 083 001

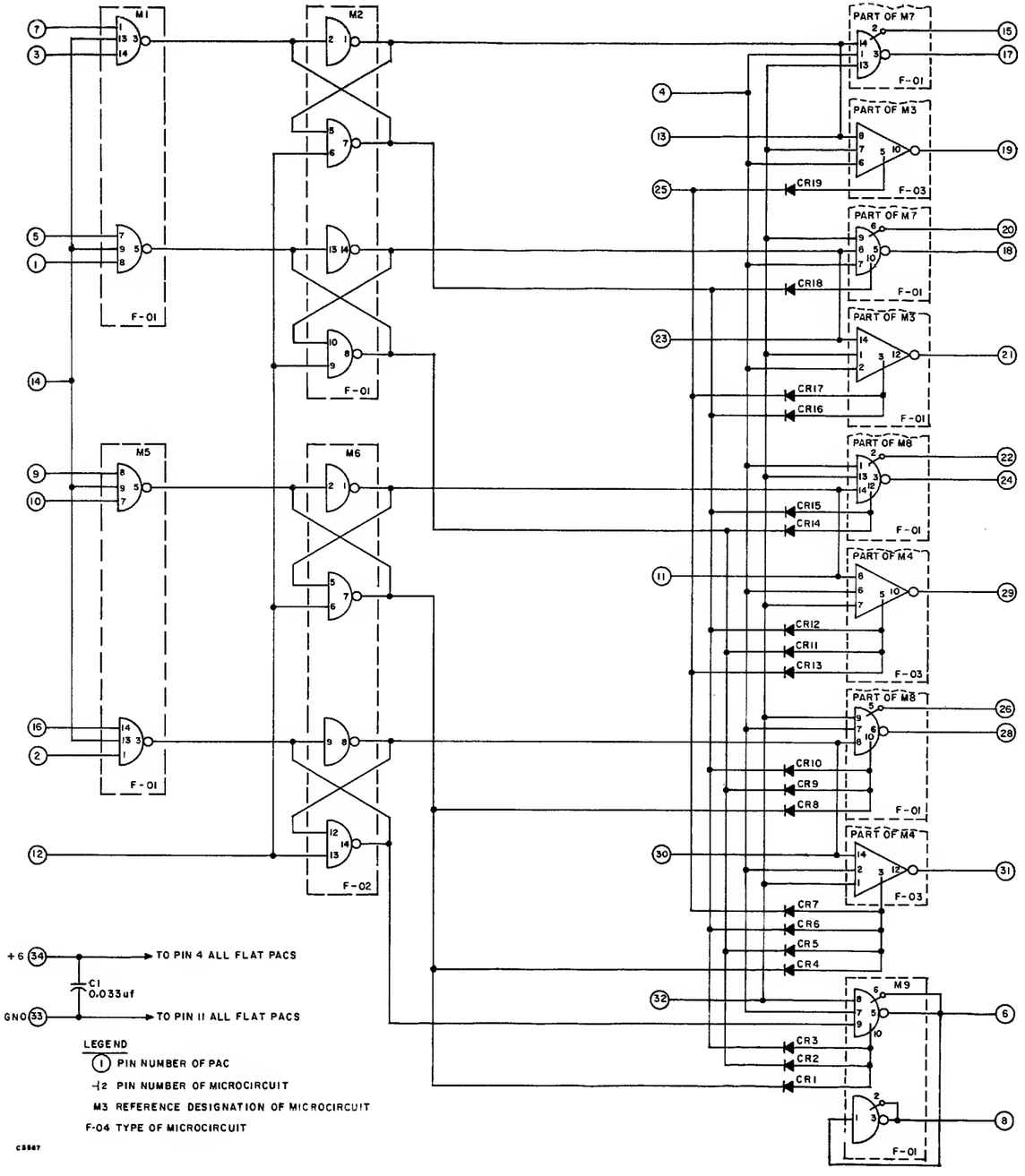


Figure A-27. Priority Pac, Model CC-044, Schematic Diagram

NAND TYPE I POWER AMPLIFIER PAC, MODEL CC-045

GENERAL DESCRIPTION

The NAND Type I Power Amplifier PAC, Model CC-045 (Figure A-28), contains three 4-input and three 2-input NAND gates that can be used to drive heavy loads. One of the 2-input gates has a node connected to pin 7 which can be used for input expansion. A three-diode cluster is also provided for expansion of input gating. Built-in short circuit protection limits the output current if the output is accidentally grounded.

CIRCUIT FUNCTION

Each gate performs the NAND function for positive logic and the NOR function for negative logic. When all inputs to a gate are positive or not connected, the output will be at ground. If any input is at ground, the output goes to a positive voltage.

NOTE

The following pins must be jumpered together on the connector into which a CC-045 is inserted. These jumpers should be made as short as possible.

Pin 20 to pin 33
Pin 27 to pin 30
Pin 30 to pin 33

SPECIFICATIONS

Frequency of Operation

DC to 10 MHz

Input Loading

2 unit loads

Current Requirements

+6v - 90 ma (max)

Power Dissipation

0.54w (max)

Output Drive Capability

12 unit loads and 70 pf stray capacitance, or
25 unit loads and 250 pf stray capacitance

Circuit Delay (measured at +1.5v, averaged over two stages)

15 ns (max) with 12 unit loads and 70 pf load
30 ns (max) with 25 unit loads and 250 pf load

Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1-M3	MICROCIRCUIT: F-09, power amplifier integrated circuit	950 100 009
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 µf ±20%, 50 vdc	930 313 016
CR1-CR3	DIODE	943 083 001

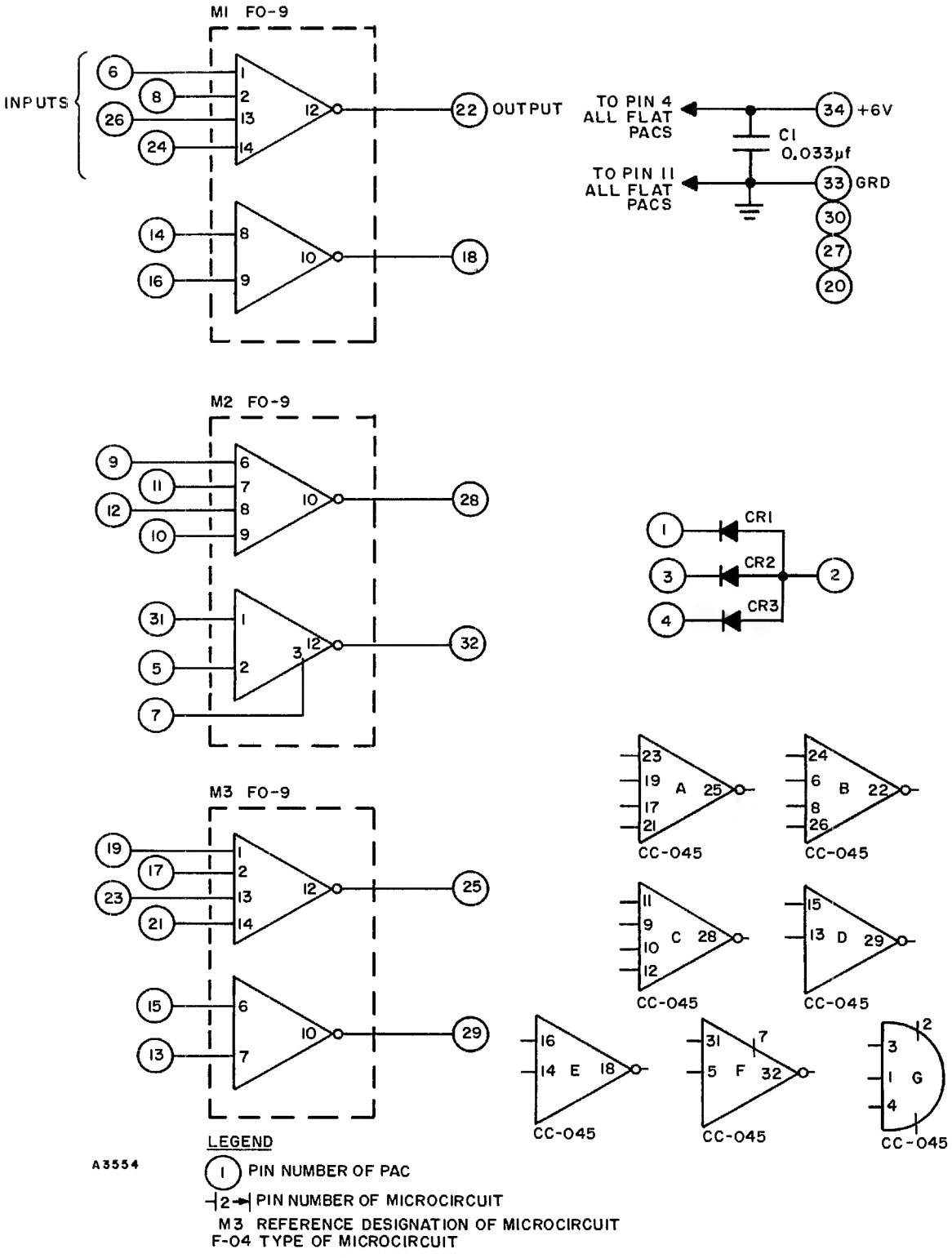


Figure A-28. NAND Type I Power Amplifier PAC, Model CC-045, Schematic Diagram and Logic Symbol

MASTER OSCILLATOR PAC, MODEL CC-046

GENERAL DESCRIPTION

The Master Oscillator PAC, Model CC-046, is a signal generator providing three output signals. Each of these outputs is timed relative to the others as shown in Figure A-29 and the specifications given below.

The basic oscillator (see Figure A-30) is comprised of two lumped constant delay lines in series with three F-09 power amplifier circuits. Taps placed on delay line DL1 are spaced at 11-ns intervals and DL2 taps are spaced 7 ns apart. The half-sections on each end of the delay lines have a delay equal to one-half the full tap delay. Outputs are provided on pins 7 and 21 for fanout expansion.

Pin 2 is an inhibit input which, when it is active, will inhibit the oscillator. When the inhibit signal goes passive, the timing cycle will start at the point indicated in Figure A-28.

NOTE

This PAC requires two slots in a solderless-wrap BLOC and one slot in a taper-pin BLOC.

Pins listed below should be connected together on the connector into which the PAC is to be inserted. These jumpers should be made as short as possible.

Pin 3 to Pin 33
Pin 5 to Pin 7 to Pin 33
Pin 13 to Pin 31
Pin 15 to Pin 21 to Pin 31
Pin 23 to Pin 29

SPECIFICATIONS

Frequency of Operation	Current Requirements
4.16 mc nominal	+6v: 100 ma (max)
Input Loading	Power Dissipation
Pin 2: 2 unit loads	600 mw (max)

Output Drive Capability

Pins 6 and 8 combined:	25 unit loads
Pins 10 and 12 combined:	25 unit loads
Pins 14 and 16 combined:	25 unit loads
Pins 18 and 20 combined:	25 unit loads
Pins 24 and 26 combined:	25 unit loads
Pin 4:	4 unit loads
Pin 22:	4 unit loads

Timing (Refer to Figure A-29)

T1, T2, T3	=	120 ±4 ns
T4, T6	=	90 ±4 ns
T5	=	14 ±4 ns
T7	=	17 ±4 ns

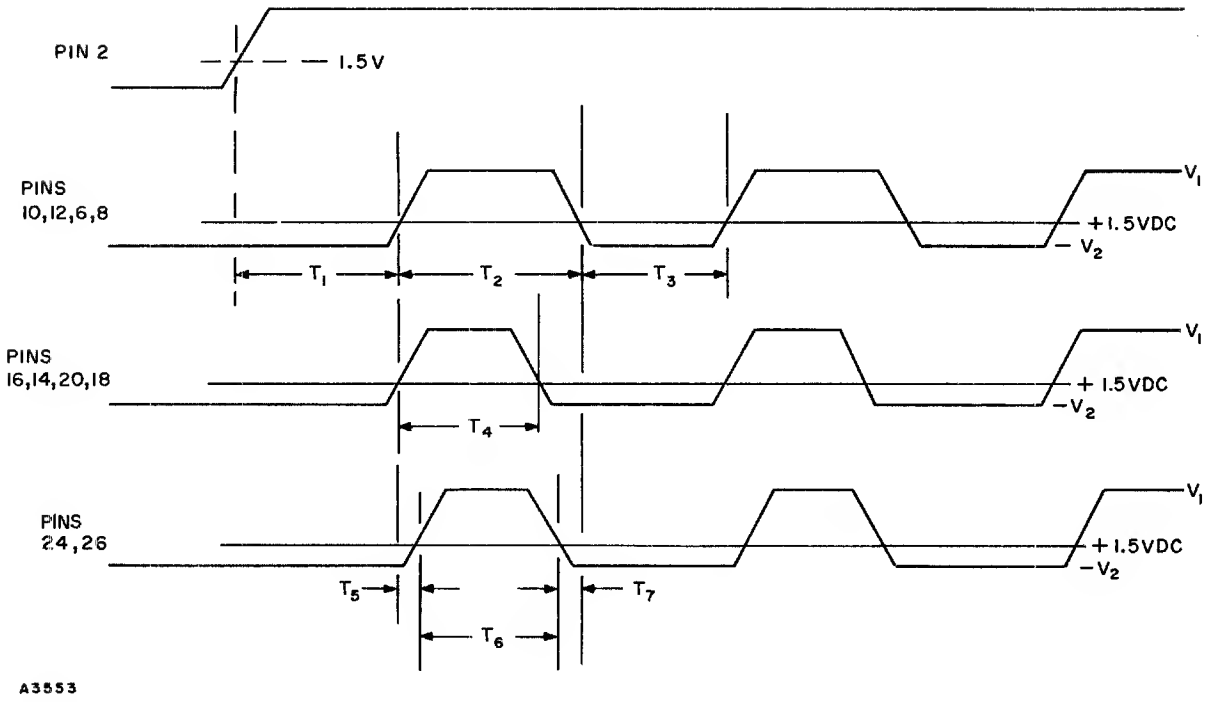


Figure A-29. Master Oscillator PAC, Model CC-046, Timing Diagram

Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1-M5	MICROCIRCUIT: F-09 power amplifier integrated circuit	950 100 009
C1-C8	CAPACITOR, FIXED, MICA DIELECTRIC: 90 pf ±2%, 100 vdc	930 004 216
C9-C16	CAPACITOR, FIXED, MICA DIELECTRIC: 38 pf ±2%, 100 vdc	930 004 207
C17	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±2%, 50 vdc	930 313 016
L1, L2	DELAY LINE	B000 206 703
R1, R2	RESISTOR, FIXED, COMPOSITION: 150 ohms ±5%, 1/2w	932 004 029
R3	RESISTOR, FIXED, COMPOSITION: 120 ohms ±5%, 1/4w	932 007 027
R4	RESISTOR, FIXED, COMPOSITION: 180 ohms ±5%, 1/4w	932 007 031

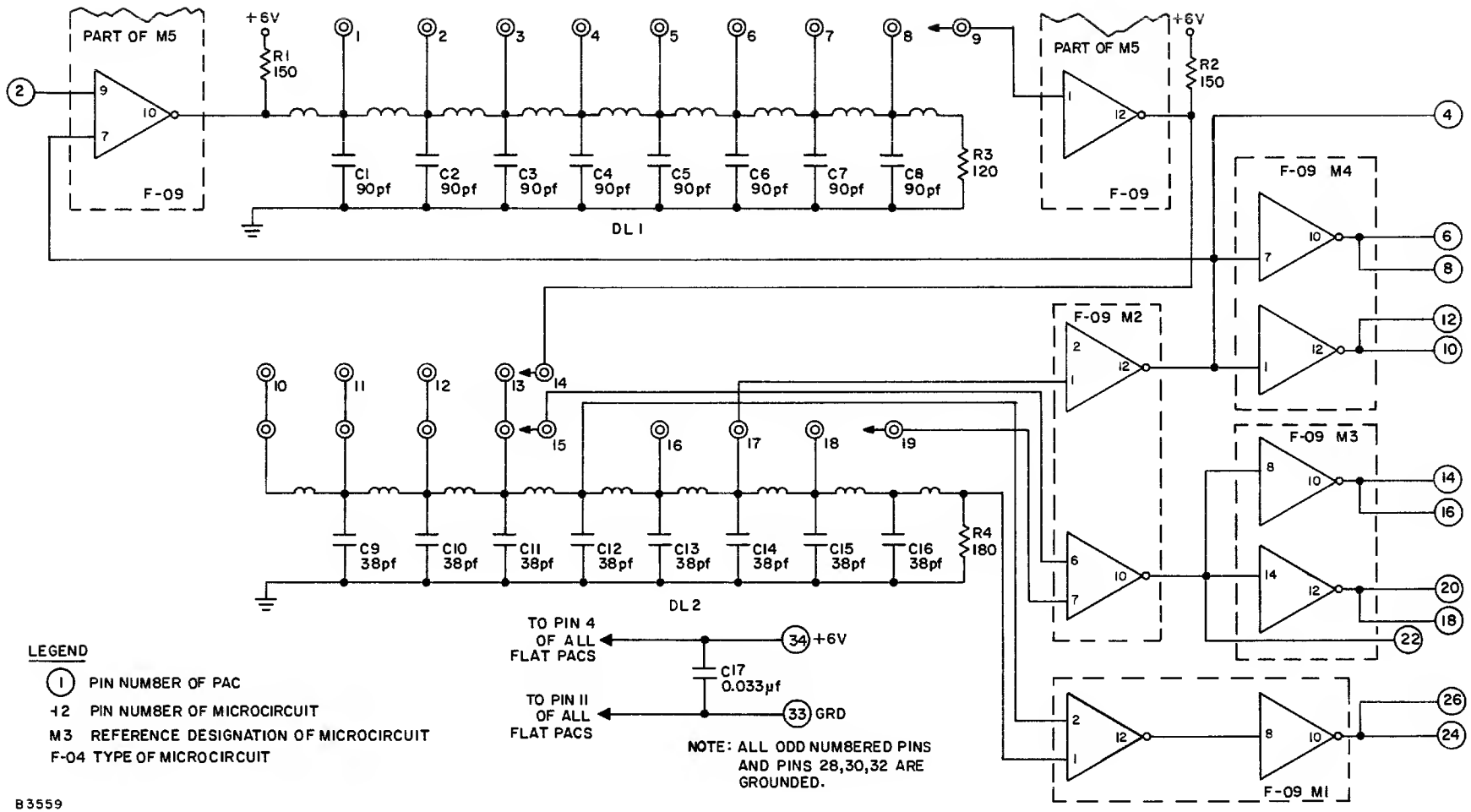


Figure A-30. Master Oscillator PAC, Model CC-046, Schematic Diagram

PIN JUMPER PAC, MODEL CC-054

GENERAL DESCRIPTION

The Pin Jumper PAC, Model CC-054, contains no components and has the following pins connected via etch.

Pin 1-3	Pin 2-4
5-7	6-8
9-11	10-12
13-15	14-16
17-19	18-20
21-23	22-24
25-27	26-28
29-31	30-32

ASR INTERFACE PAC, MODEL CC-057

GENERAL DESCRIPTION

The ASR Interface PAC, Model CC-057 (Figure A-31) contains a single bidirectional circuit for interfacing with ASR signals. In one mode, standard μ-PAC signals are applied to input pins 14 and 16, and the CC-057 functions as an OR circuit. If either or both of the inputs is passive, pin 22 will sink 60 ma (nominal) from a +24v supply. When both inputs are active, the current drops to below 3 ma.

In the other mode, the presence or absence of a 24v level at pin 22 is indicated by an output at pin 25 of active or passive, respectively.

NOTE

The CC-057 requires two slots in a solderless-wrap BLOC.

SPECIFICATIONS

Frequency of Operation

DC to 100 Hz

Input Loading

Pins 14 and 16: 1-1/2 unit loads each

Output Drive Capability

Pin 22: sink 60 ma from +24v supply

Pin 25: 2 unit loads

Current Requirements

+6v: 13 ma

Power Dissipation

0.08w

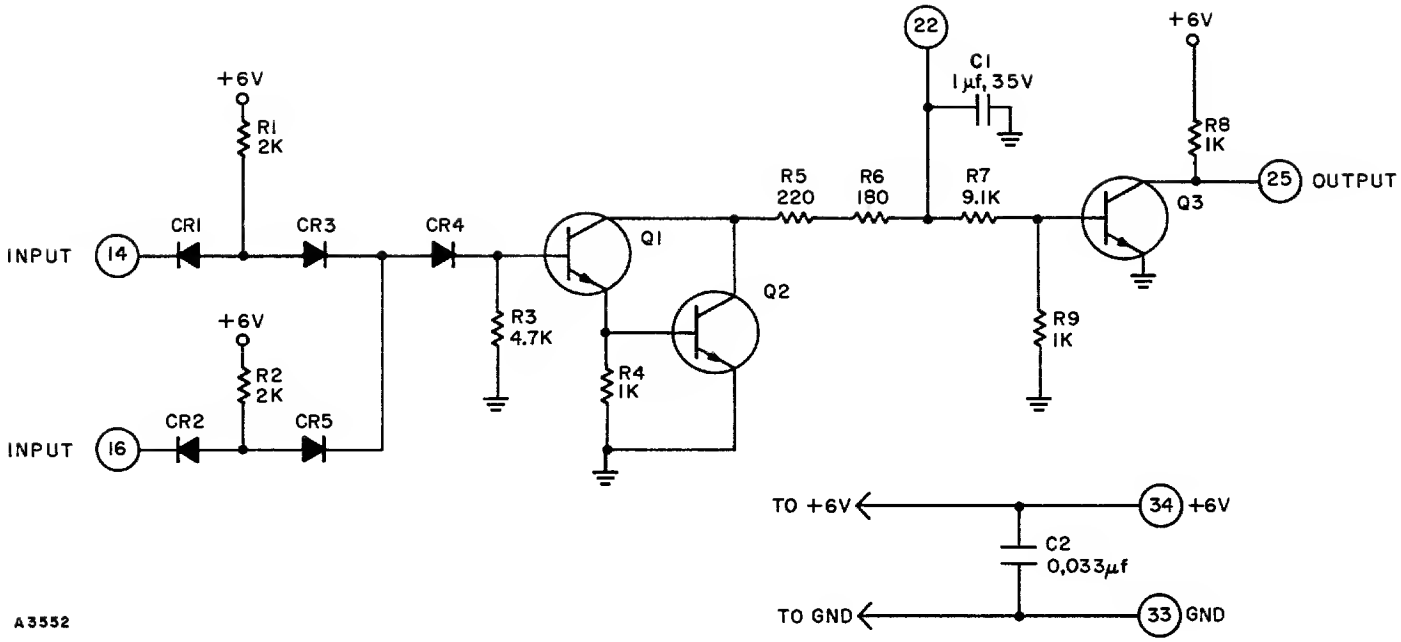


Figure A-31. ASR Interface PAC, CC-057, Schematic Diagram

Electrical Parts List

Ref. Desig.	Description	3C Part No.
C1	CAPACITOR, FIXED, TANTALUM: 1.0 µf ±10%, 35 vdc	930 217 054
C2	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 µf ±20%, 50 vdc	930 313 016
CR1-CR5	DIODE	943 083 001
Q1, Q2	TRANSISTOR: Replacement Type 2N2369	943 720 001
Q3	TRANSISTOR: Replacement Type 2N3011	943 722 002
R1, R2	RESISTOR, FIXED, COMPOSITION: 2 K ±5%, 1/4w	932 007 056
R3	RESISTOR, FIXED, COMPOSITION: 4.7 K ±5%, 1/4w	932 007 065
R4, R8, R9	RESISTOR, FIXED, COMPOSITION: 1 K ±5%, 1/4w	932 007 049
R5	RESISTOR, FIXED, COMPOSITION: 220 ohms ±5%, 2w	932 006 033
R6	RESISTOR, FIXED, COMPOSITION: 180 ohms ±5%, 2w	932 006 031
R7	RESISTOR, FIXED, COMPOSITION: 9.1 K ±5%, 1/4w	932 007 072

NAND TYPE II POWER AMPLIFIER PAC, MODEL CC-073

GENERAL DESCRIPTION

The NAND Type II Power Amplifier PAC, Model CC-073 (Figure A-32), contains six 3-input NAND gates that can be used to drive heavy loads. One of the gates has a node connected to pin 8 which can be used for input expansion. A three-diode cluster is also provided for expansion of input gating. Built-in short circuit protection limits the output current if the output is accidentally grounded.

CIRCUIT FUNCTION

Each gate performs the NAND function for positive logic and the NOR function for negative logic. When all inputs to a gate are positive or not connected, the output will be at ground. If any input is at ground, the output goes to a positive voltage.

NOTE

The following pins must be jumpered together on the connector into which a CC-073 is inserted. These jumpers should be made as short as possible.

From pin 18 to pin 33
From pin 25 to pin 28
From pin 28 to pin 33

SPECIFICATIONS

Frequency of Operation

DC to 10 MHz

Output Drive Capability

12 unit loads and 70 pf stray, or
25 unit loads and 250 pf stray

Input Loading

2 unit loads

Current Requirements

+6v: 90 ma (max)

Power Dissipation

0.54w (max)

Circuit Delay (measured at +1.5v, averaged over two stages)

15 ns (max) with 12 unit loads and 70 pf load
30 ns (max) with 25 unit loads and 250 pf load

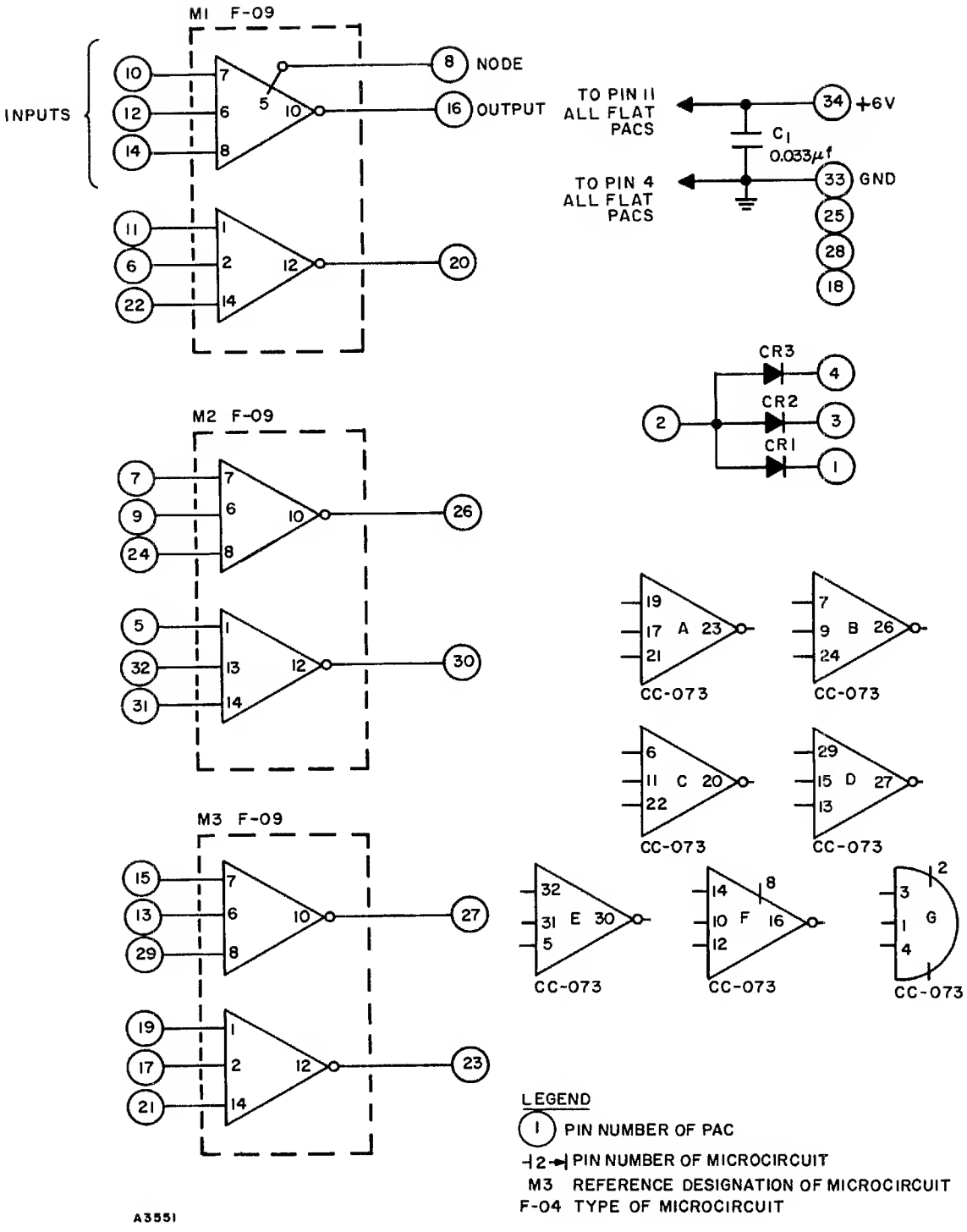


Figure A-32. NAND Type II Power Amplifier PAC, Model CC-073, Schematic Diagram and Logic Symbols

Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1-M3	MICROCIRCUIT: F-09, power amplifier integrated circuit	950 100 009
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
CR1-CR3	DIODE	943 083 001

MULTIVIBRATOR CLOCK PAC, MODEL CC-074

GENERAL DESCRIPTION

The Multivibrator Clock PAC, Model CC-074 (Figure A-33), contains a self-starting, free-running multivibrator, a pulse shaper and a pulse amplifier. Frequency of operation is preset to 440 Hz at the factory. The PAC is prewired to provide negation pulses through a standard power amplifier microcircuit. In addition, an oscillator inhibit is internally wired to provide synchronous start/stop capability from external asynchronous signals. The oscillator is inhibited by a passive level and enabled by an active level. The PAC also contains an independent power amplifier.

NOTE

The oscillator inhibit (pin 9) must be at ground in order to generate pulses.

CIRCUIT FUNCTION

Multivibrator Circuit

The multivibrator is a self-starting, free-running circuit with an operating frequency range between 0 and 5 mc. Potentiometer R10 permits continuous variation within the range. However, R10 is preset at 440 Hz and then epoxied to prevent frequency deviations because of readjustment or vibration.

Pulse Shaper Circuit

The pulse shaper is a current-mode, non-saturating circuit which is dc-coupled at the multivibrator by transistor Q6. Pulse widths can be varied by means of a built-in potentiometer-capacitor network. Potentiometer R17 can be used to make pulse width adjustment between 1 and 5 μsec.

Gated Input

This point is a power amplifier microcircuit input. When the gated input is passive, or not connected, pulses from the oscillator will appear at the output. When the input is active, output pulses are inhibited.

Oscillator Inhibit

When the oscillator inhibit input makes a transition to ground, a pulse will be generated at the PAC output within 200 ns of the transition.

NOTE

The CC-074 PAC occupies two slots in a solderless-wrap μ-BLOC.

SPECIFICATIONS

Current Requirements

+6v: 110 ma (max)

-6v: 50 ma (max)

Power Dissipation

0.96w (max)

Multivibrator Circuit

Input Loading

Gated input: 2 unit loads

Frequency

440 ±1 Hz

Output Drive Capability

25 unit loads

Pulse Width Stability

Temperature 0°C to +50°C: ±10% (max)

Voltage ±5%: ±5% (max)

Frequency Stability

Temperature 0°C to +50°C: ±1% (max)

Voltage variation ±5%: ±2% (max)

Overall stability: ±4% (max)

Circuit Delay (Measured at +1.5v, averaged over two stages):

30 ns (max)

Power Amplifier

Frequency of Operation (System)

DC to 5MHz

Input Loading

2 unit loads each

Output Drive Capability

25 unit loads

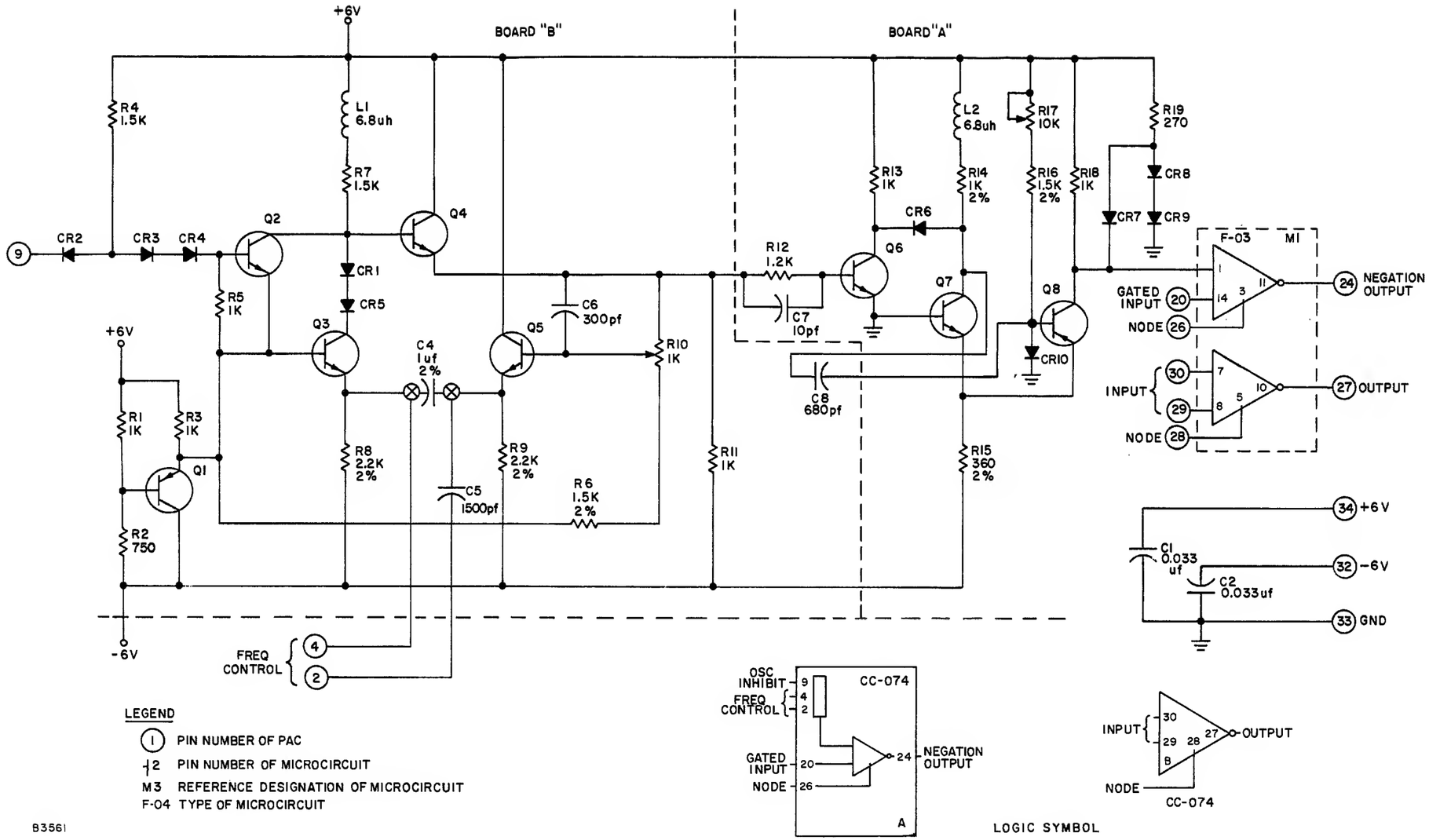


Figure A-33. Multivibrator Clock PAC Model CC-074, Schematic Diagram

Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1	MICROCIRCUIT: F-03 power amplifier integrated circuit	950 100 003
C1,C2	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
C3	Deleted	
C4	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 1.0 μf ±2%, 50 vdc	930 316 037
C5	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 1500 pf ±5%, 50 vdc	930 313 205
C6	CAPACITOR, FIXED, MICA DIELECTRIC: 300 pf ±2%, 100 vdc	930 005 534
C7	CAPACITOR, FIXED, DIELECTRIC: 10 pf ±5%, 75 vdc	930 700 202
C8	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 680 pf ±10%, 50 vdc	930 313 102
CR1-CR9	DIODE: Replacement Type 1N914	943 083 001
CR10	DIODE: Replacement Type FD777	943 088 001
L1,L2	COIL, R.F.: 6.8 μh ±10%	939 207 023
R1,R3,R5,R11, R13,R18	RESISTOR, FIXED, COMPOSITION: 1K ±5%, 1/4w	932 007 049
R2	RESISTOR, FIXED, COMPOSITION: 750 ohms ±5%, 1/4w	932 007 046
R4,R7,R12	RESISTOR, FIXED, COMPOSITION: 1.5 K ±5%, 1/4w	932 007 053
R6,R16	RESISTOR, FIXED, FILM: 1.5 K ±2%, 1/4w	932 114 053
R8,R9	RESISTOR, FIXED, FILM: 2.2 K ±2%, 1/4w	932 114 057
R10	RESISTOR, VARIABLE, FILM: 1 K ±10%, 3/4w	933 300 104
R14	RESISTOR, FIXED, FILM: 1 K ±2%, 1/4w	932 114 049
R15	RESISTOR, FIXED, FILM: 360 ohms ±2%, 1/4w	932 114 038
R17	RESISTOR, VARIABLE, FILM: 10 K ±10%, 3/4w	933 300 107
R19	RESISTOR, FIXED, COMPOSITION: 270 ohms ±5%, 1/4w	932 007 035
Q1	TRANSISTOR: Replacement Type 2N3012	943 721 002
Q2-Q8	TRANSISTOR:	943 722 002

CABLE PAC, MODEL CC-079

GENERAL DESCRIPTION

The Cable PAC, Model CC-079 (Figure A-34), terminates 32 twisted pairs of a cable. The source of the signals terminating to and from the PAC are from components mounted in the control panel and main frame logic of a computer. Noise protection is provided by the resistor terminations for passive signals. One end of each resistor is connected to +6v, thus placing an otherwise floating signal at +6v.

Electrical Parts List

Ref. Desig.	Description	3C Part No.
C1	CAPACITOR, FIXED, ELECTROLYTIC: 2.2 μf ±20%, 35 vdc	930 217 017
R1-R16	RESISTOR, FIXED, COMPOSITION: 1 K ±5%, 1/4w	932 007 049

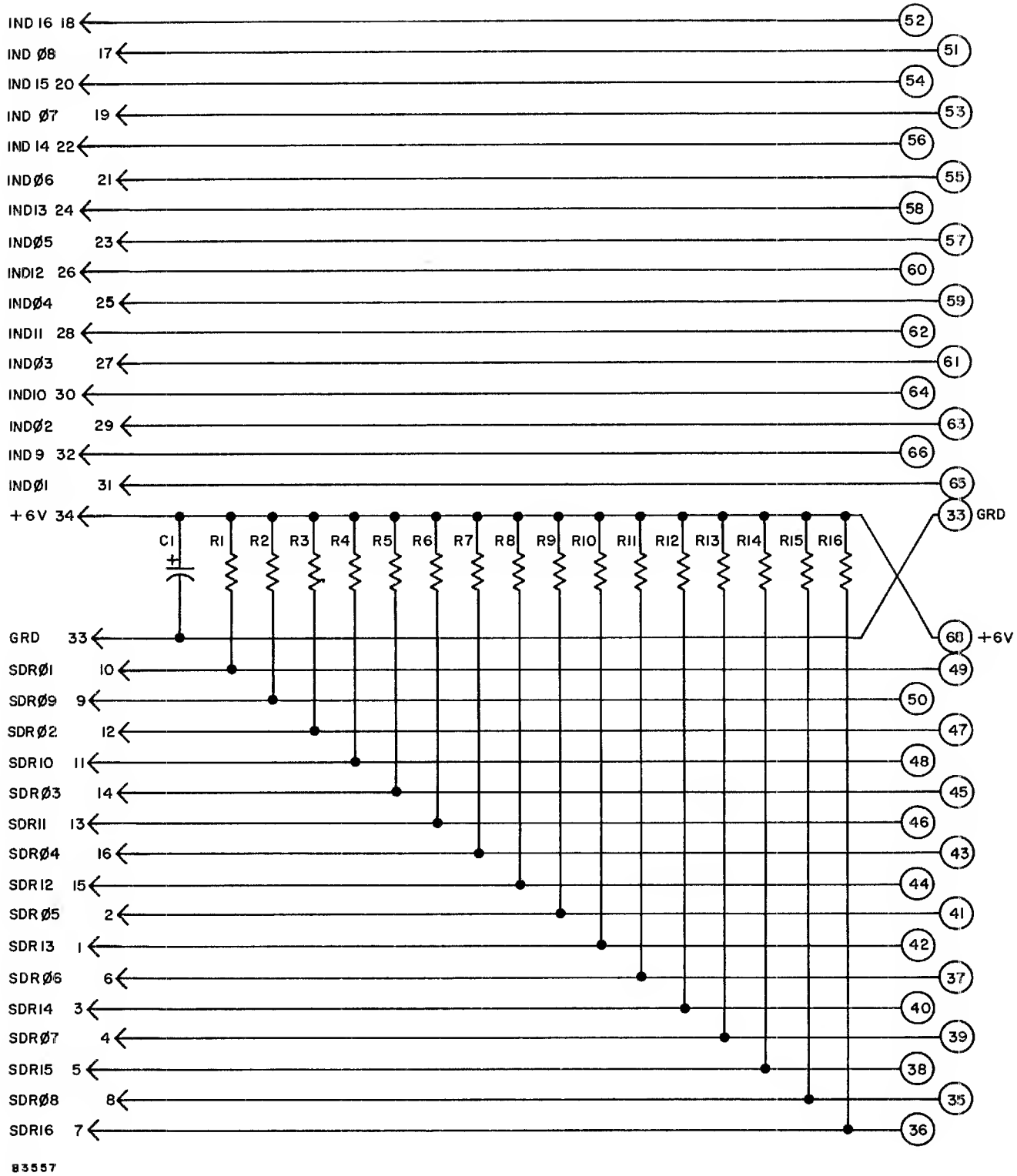


Figure A-34. Cable PAC, Model CC-079, Schematic Diagram

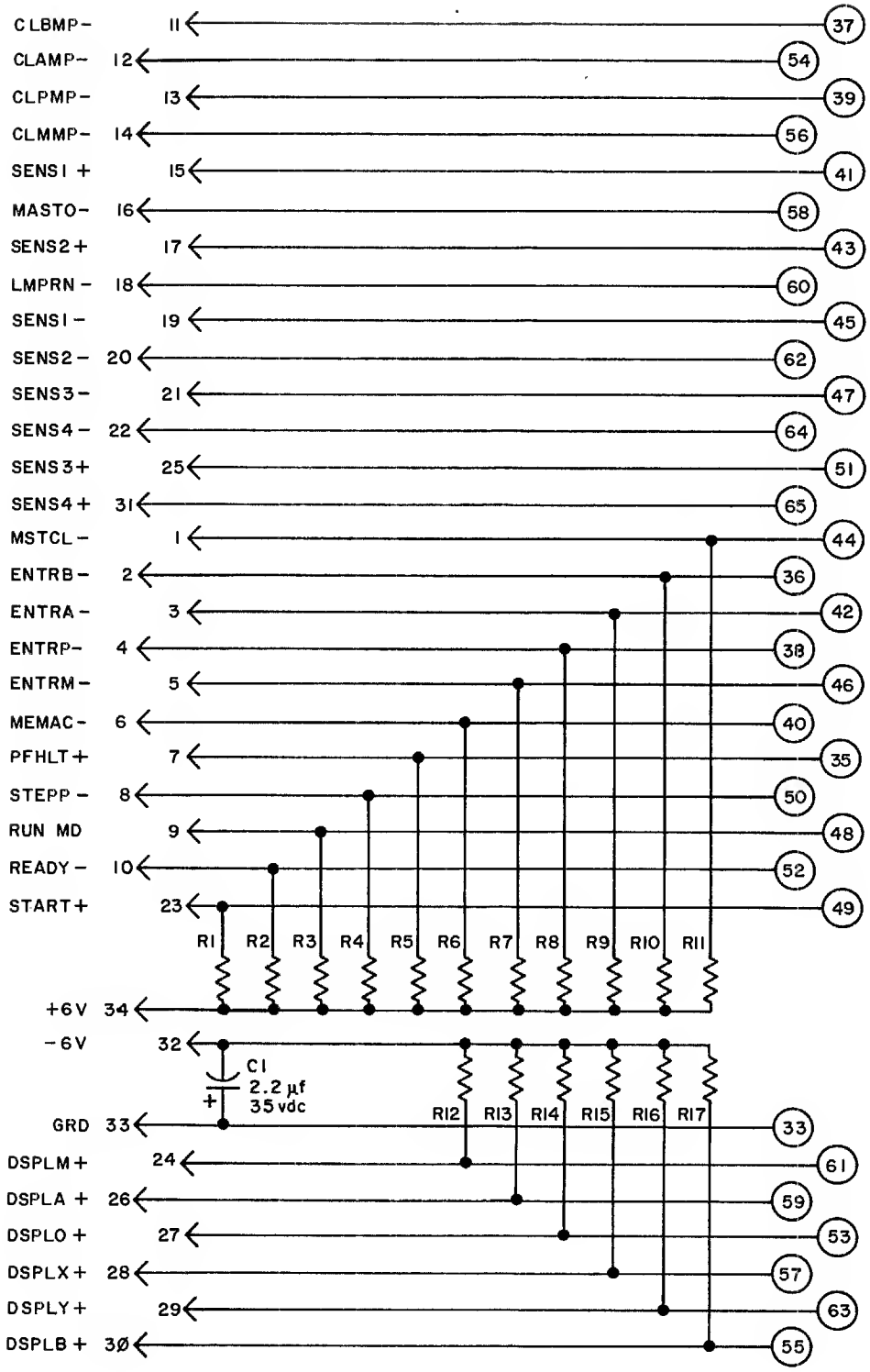
CABLE PAC, MODEL CC-080

GENERAL DESCRIPTION

The Cable PAC, Model CC-080 (Figure A-35), terminates 32 twisted pairs of a cable. The source of the signals terminating to and from the PAC are from components mounted in the control panel and main frame logic of a computer. Noise protection is provided by the resistor terminations for open circuits. One end of each resistor is connected to +6v, thus placing an otherwise floating signal at +6v.

Electrical Parts List

Ref. Desig.	Description	3C Part No.
C1	CAPACITOR, FIXED, ELECTROLYTIC: 2.2 µf ±20%, 35 vdc	930 217 017
R1-R17	RESISTOR, FIXED, COMPOSITION: 1 K ±5%, 1/4w	932 007 049



A3560

Figure A-35. Cable PAC, Model CC-080, Schematic Diagram

UNIVERSAL FLIP-FLOP PAC, MODEL CC-085

The Universal Flip-Flop PAC, Model CC-085 (Figures A-36 and A-37), contains three versatile, independent flip-flops which can perform the functions of storage, counting, shifting, and control. Each flip-flop circuit has a comprehensive input structure which allows control of the flip-flop from a variety of level and pulse inputs. Each stage has two dc set and two dc reset inputs, set control and reset control inputs, a clock input, and set and reset outputs. There is also a common reset input for clearing all stages simultaneously.

INPUT AND OUTPUT SIGNALS

DC Set and DC Reset. -- A signal at ground from 80 nsec or longer on any dc set or reset input will set or reset the flip-flop, respectively.

Common Reset. -- A signal at ground for 80 nsec or longer on the common reset input clears the three stages simultaneously.

Set Control and Reset Control. -- +6v is the enabling level on the control inputs. Refer to Section II for complete information on flip-flop operation.

Clock. -- The flip-flop can change state on the negative transition on the clock input.

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 mc

Input Loading

DC inputs:	2/3 unit load each
Control inputs:	1 unit load each
Clock input:	1 unit load each
Common input:	1 unit load each
Common reset:	2 unit lods

Output Drive Capability

8 unit loads

Circuit Delay

Clock input to set or reset output:
60 nsec (max)

DC set input to set output, or dc reset input to reset output:
80 nsec (max)

DC set input to reset output, or dc reset input to set output:
60 nsec (max)

Current Requirements

+6v: 75 ma (max)

Power Dissipation

0.45w (max)

Handle Color Code

Blue

APPLICATIONS

The CC-085 PAC can be used as a counter (Figures A-38 and A-39) or as a shift register (Figure A-40). The method of parallel information drop-in is illustrated in Figure A-41.

Data may be transferred to the flip-flop with single-ended signals by first resetting all stages, then setting only the appropriate ones. With double-ended data transfer, complementary signals are applied to the dc set and dc reset inputs for putting the flip-flop in the appropriate state in one operation.

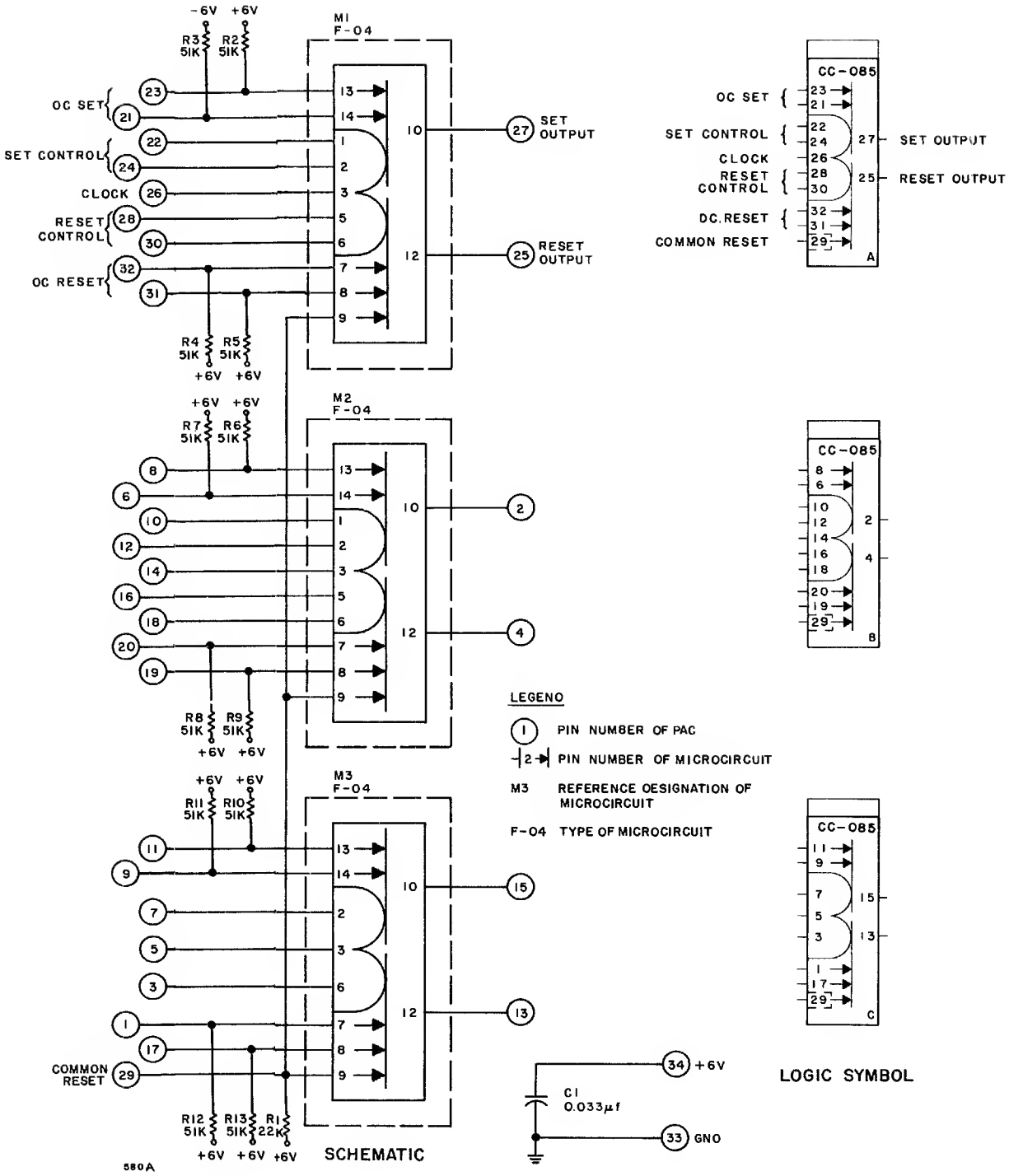
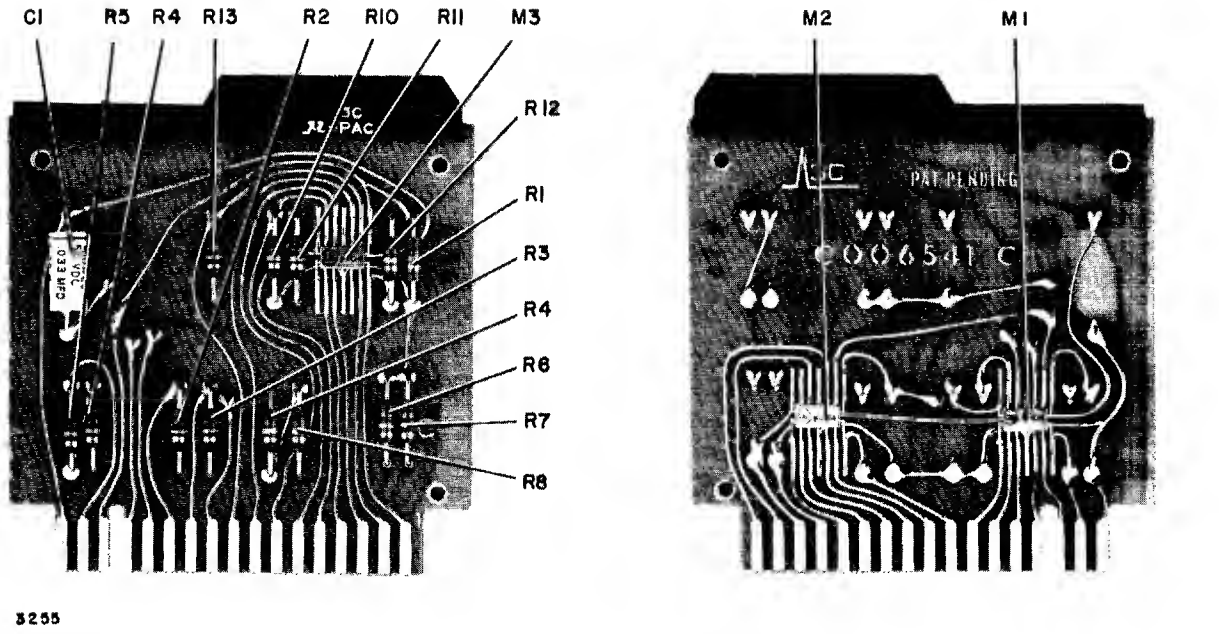


Figure A-36. Universal Flip-Flop PAC, Model CC-085, Schematic Diagram and Logic Symbol

Parts Location



Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1-M3	MICROCIRCUIT: F-04, flip-flop integrated circuit	950 100 044
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 µf, ±20%, 50 vdc	930 313 016
R1	RESISTOR, FIXED, COMPOSITION: 22K ±5%, 1/4w	932 007 081
R2-R13	RESISTOR, FIXED, COMPOSITION: 51K ±5%, 1/4w	932 007 090

Figure A-37. Universal Flip-Flop PAC, Model CC-085, Parts Location and Identification

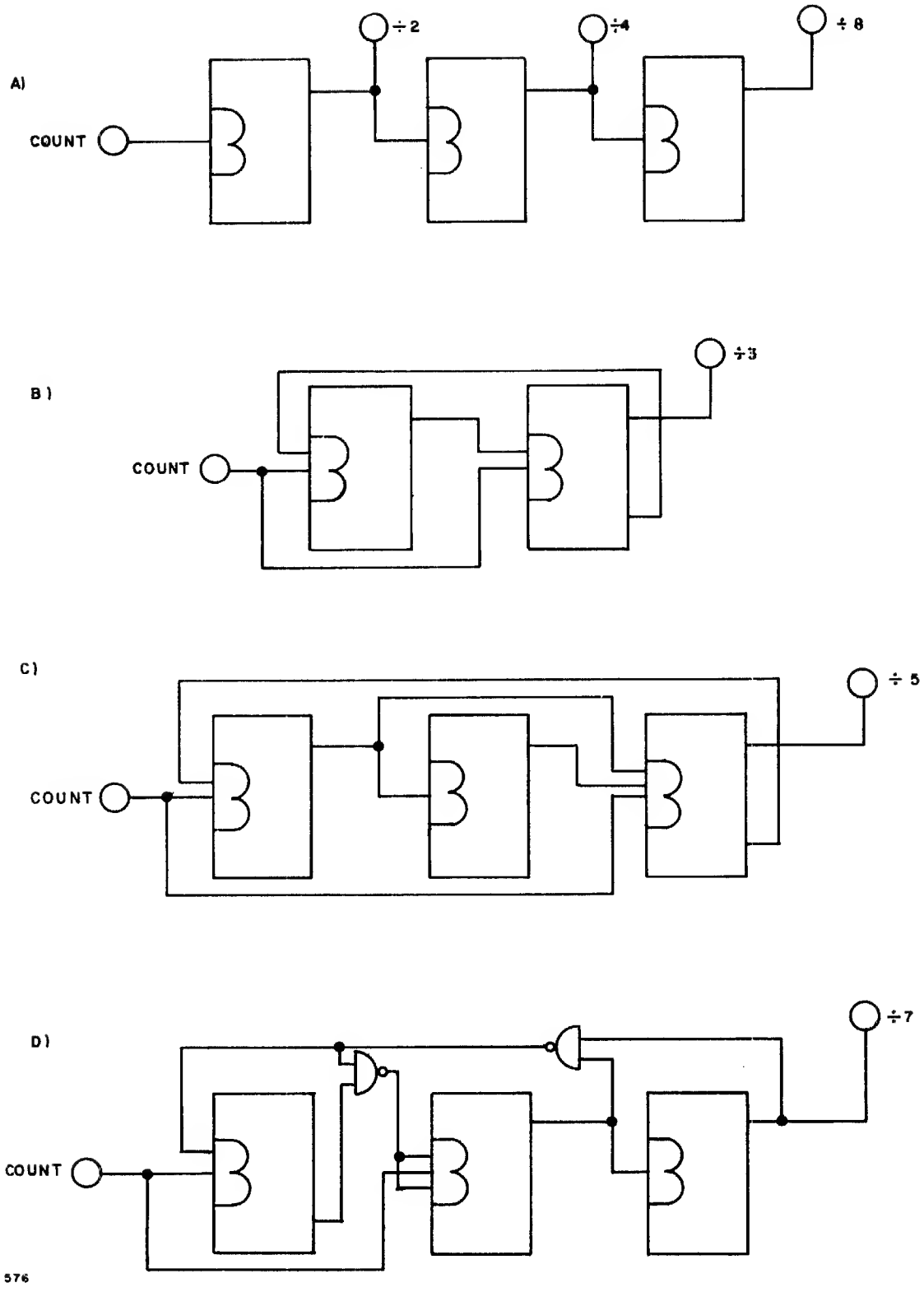


Figure A-38. Universal Flip-Flop PAC, Model CC-085, Counter Operation

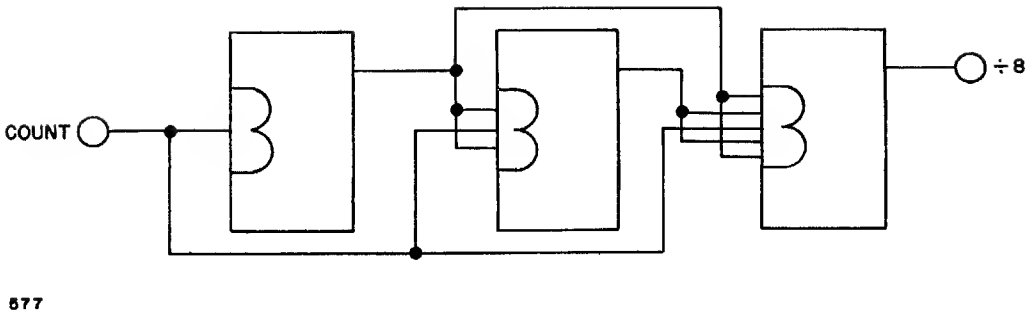


Figure A-39. Universal Flip-Flop PAC, Model CC-085, Three-Stage Instantaneous Carry Operation

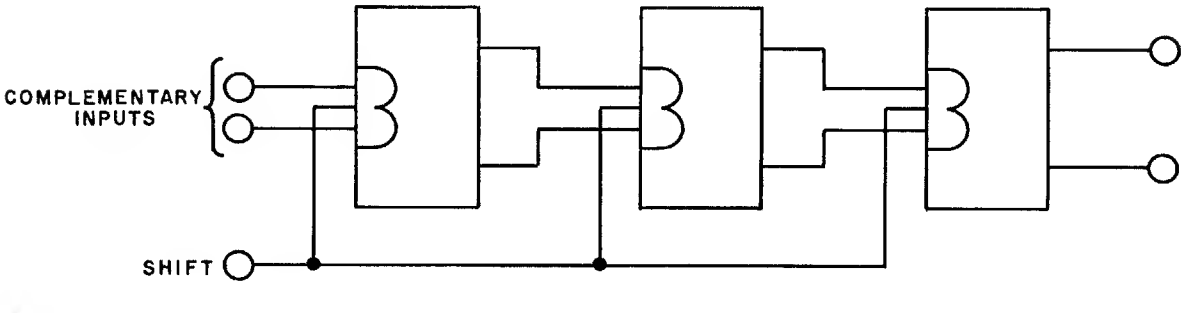


Figure A-40. Universal Flip-Flop PAC, Model CC-085, Shift Register Operation

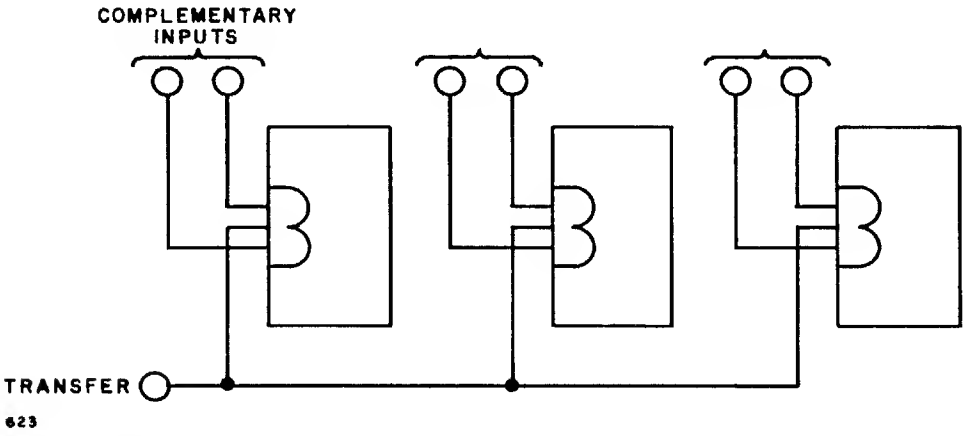


Figure A-41. Universal Flip-Flop PAC, Model CC-085, Parallel Information Drop-In

GATED FLIP-FLOP PAC, MODEL CC-086

The Gated Flip-Flop PAC, Model CC-086 (Figures A-42 and A-43), contains four independent flip-flops. A versatile input structure allows control from a variety of levels and pulses. Typical applications are storage, counting and shifting, and control.

INPUT and OUTPUT SIGNALS

DC Set and DC Reset. -- A signal which is at 0v for 80 nsec or longer on a dc set (or reset) input will set (or reset) the flip-flop. Circuit C will set or reset with 60 nsec.

Common Reset. -- A signal which is at 0v for 80 nsec or longer on the common reset input clears all four stages simultaneously.

Set Control and Reset Control. -- +6v is the enabling level on the control inputs. Refer to Section II for detailed information on flip-flop timing and control.

Clock. -- The flip-flop changes state on the negative transition of the clock input.

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 mc

Input Loading

DC inputs:	2/3 unit load each
Control inputs:	1 unit load each
Common reset:	3 unit loads
Clock:	1 unit load each

Output Drive Capability

8 unit loads each

Circuit Delay

Clock input to set or reset output
60 nsec (max)

DC set input to dc set output, or dc reset input to reset output
80 nsec (max)

DC set input to reset output, or dc reset input to set output
60 nsec (max)

Current Requirements

+6v: 100 ma (max)

Power Dissipation

0.60w (max)

Handle Color Code

Blue

APPLICATIONS

The CC-086 can be used as a counter (Figure A-44) or as a shift register (Figure A-45). The method of parallel information drop-in is shown in Figure A-46.

Data may be transferred to the flip-flop with a single-ended signal by first resetting all stages, then setting the appropriate ones. For double-ended data transfer, complementary signals applied to the dc set and dc reset inputs set the flip-flop to the appropriate state in one operation.

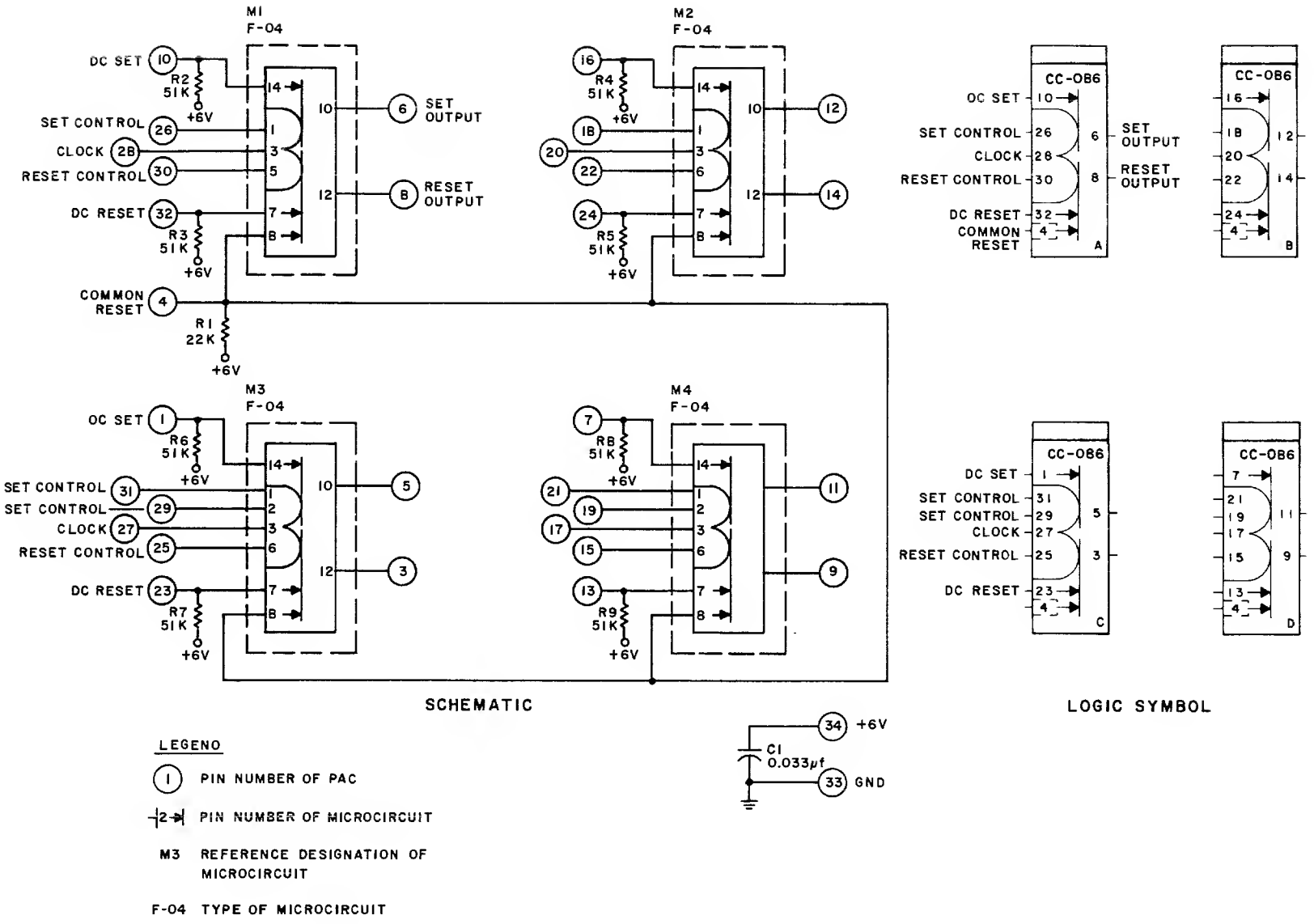
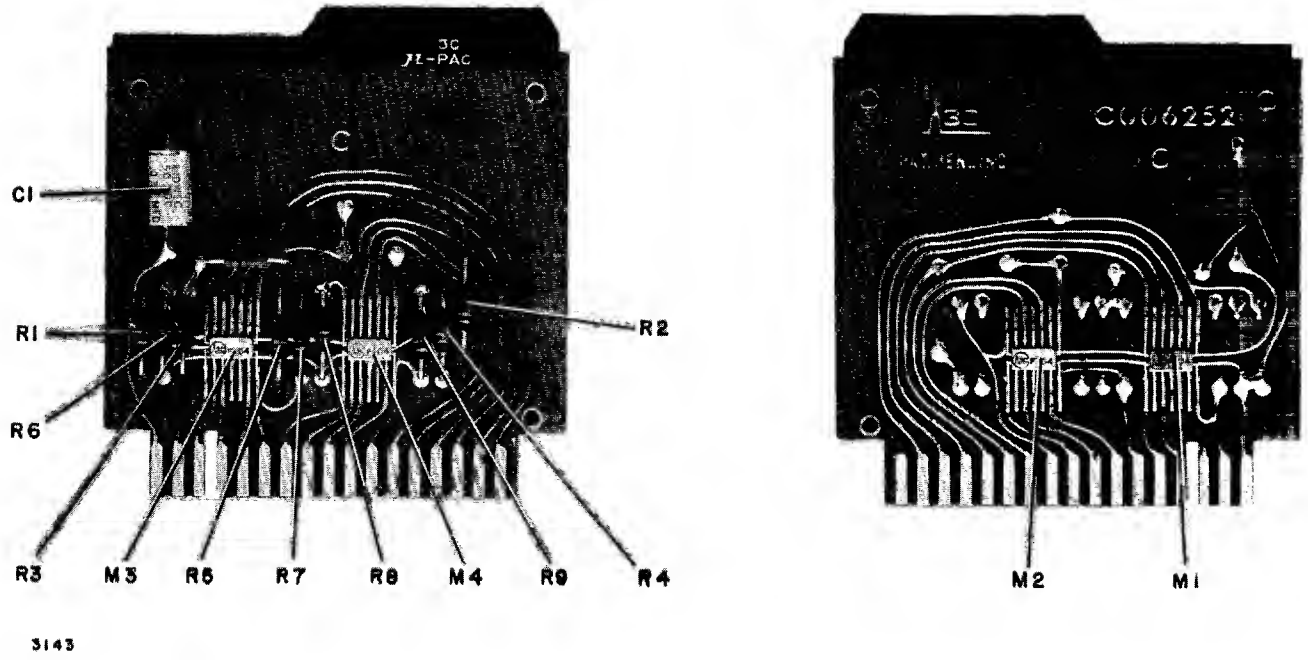


Figure A-42. Gated Flip-Flop PAC, Model CC-086, Schematic Diagram and Logic Symbol

Parts Location



Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1-M4	MICROCIRCUIT: F-04, flip-flop integrated circuit	950 100 004
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
R1	RESISTOR, FIXED, COMPOSITION: 22K ±5%, 1/4w	932 007 081
R2-R9	RESISTOR, FIXED, COMPOSITION: 51K ±5%, 1/4w	932 007 090

Figure A-43. Gated Flip-Flop PAC, Model CC-086, Parts Location and Identification

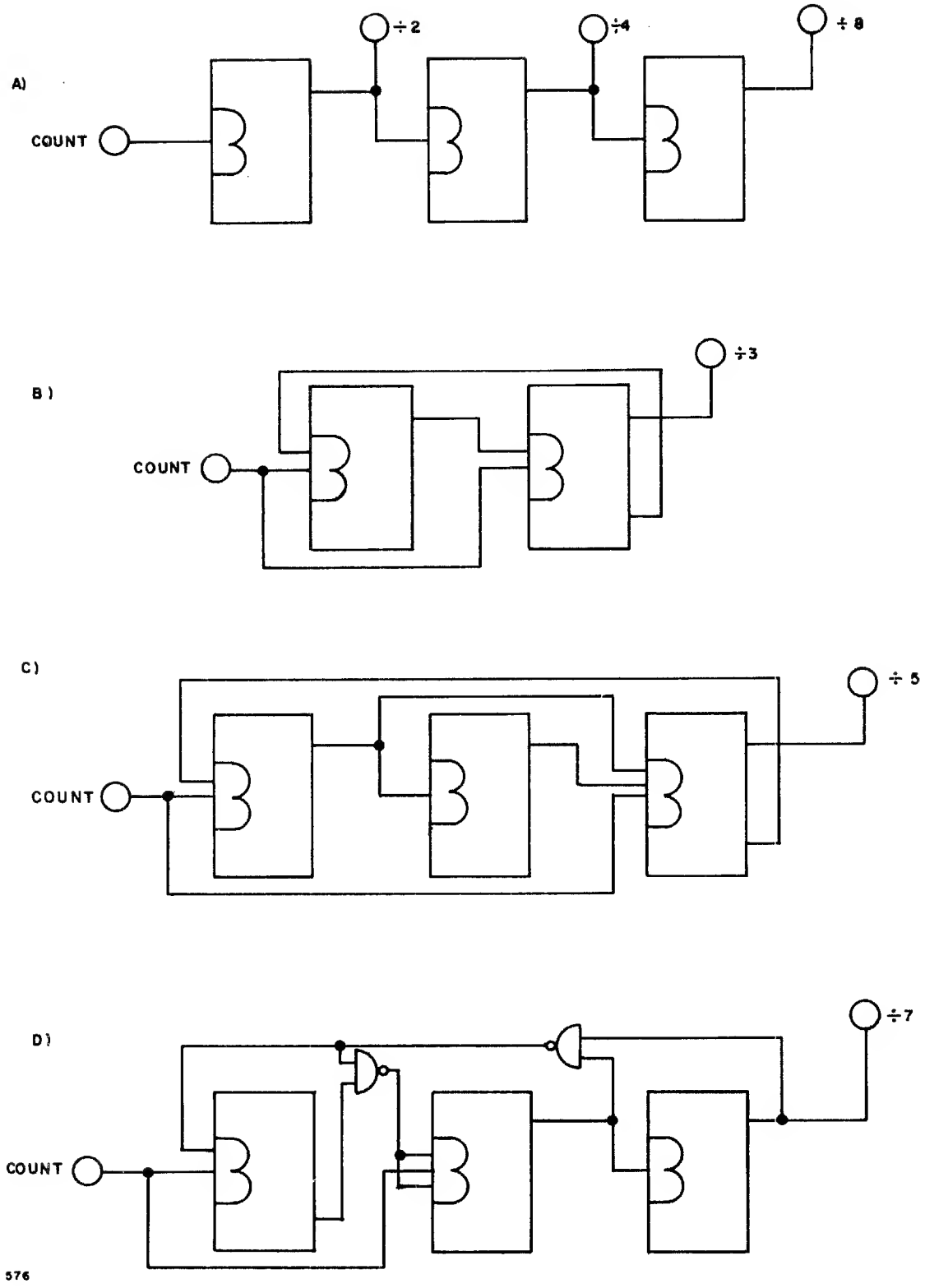


Figure A-44. Gated Flip-Flop PAC, Model CC-086, Counter Operation

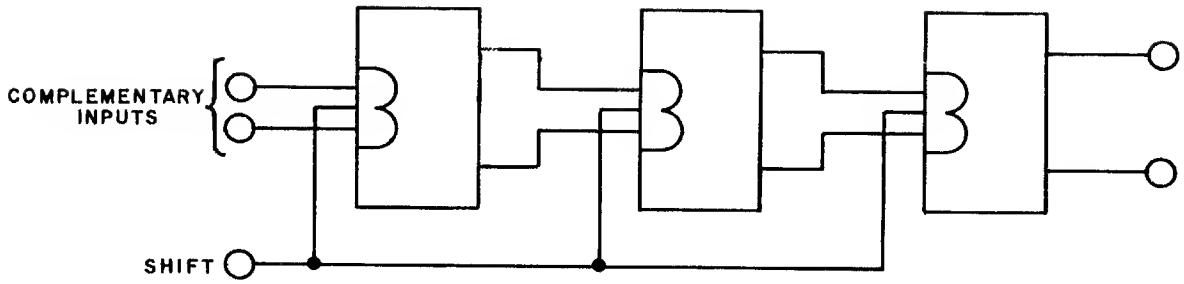


Figure A-45. Gated Flip-Flop PAC, Model CC-086, Shift Register Operation

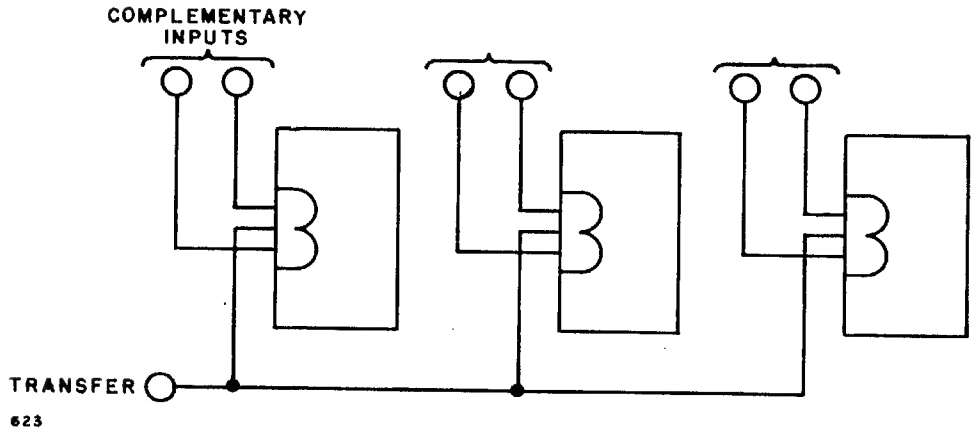


Figure A-46. Gated Flip-Flop PAC, Model CC-086, Parallel Information Drop-In

COUNTER PAC, MODEL CC-088

The Counter PAC, Model CC-088 (Figures A-47 and A-48), contains six independent flip-flops that can be used for counting, frequency division, and buffer storage. Each stage has a complement input, dc set and dc reset inputs, and set and reset outputs. There is also a common reset input for clearing all stages simultaneously. Application of a signal to the complement input causes the flip-flop to change state. (Toggling action is accomplished without additional wiring.)

INPUT AND OUTPUT SIGNALS

DC Set and Reset. -- A signal at 0v for 80 nsec or longer on the dc set (or reset) input will set (or reset) the flip-flop.

Common Reset. -- A signal at 0v for 80 nsec or longer on the common reset input will clear the six counter stages simultaneously.

Complement. -- The output changes state on the negative transition of the complement input. This input is the same as the clock input of the integrated circuit flip-flop.

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 mc

Input Loading

DC inputs:	2/3 unit load each
Common reset:	4 unit loads
Complement:	1 unit load each

Output Drive Capability

8 unit loads each

Handle Color Code

Blue

Circuit Delay

Complement input to flip-flop outputs (counter propagation stage delay): 60 nsec (max)

DC set input to set output, or dc reset input to reset output: 80 nsec (max)

DC set input to reset output, or reset input to set ouput: 60 nsec(max)

Current Requirements

+6v: 150 ma (max)

Power Dissipation

0.90w (max)

APPLICATIONS

Each of the stages can be used separately for divide-by-two, complementing operation. Successively connecting the set output of one stage to the complement input of another stage (Figure A-49) results in frequency division by factors of 4, 8, 16, 32 or 64. In this configuration, the PAC has a capacity as a counter of 0 through $2^6 - 1$, a total of 64 states.

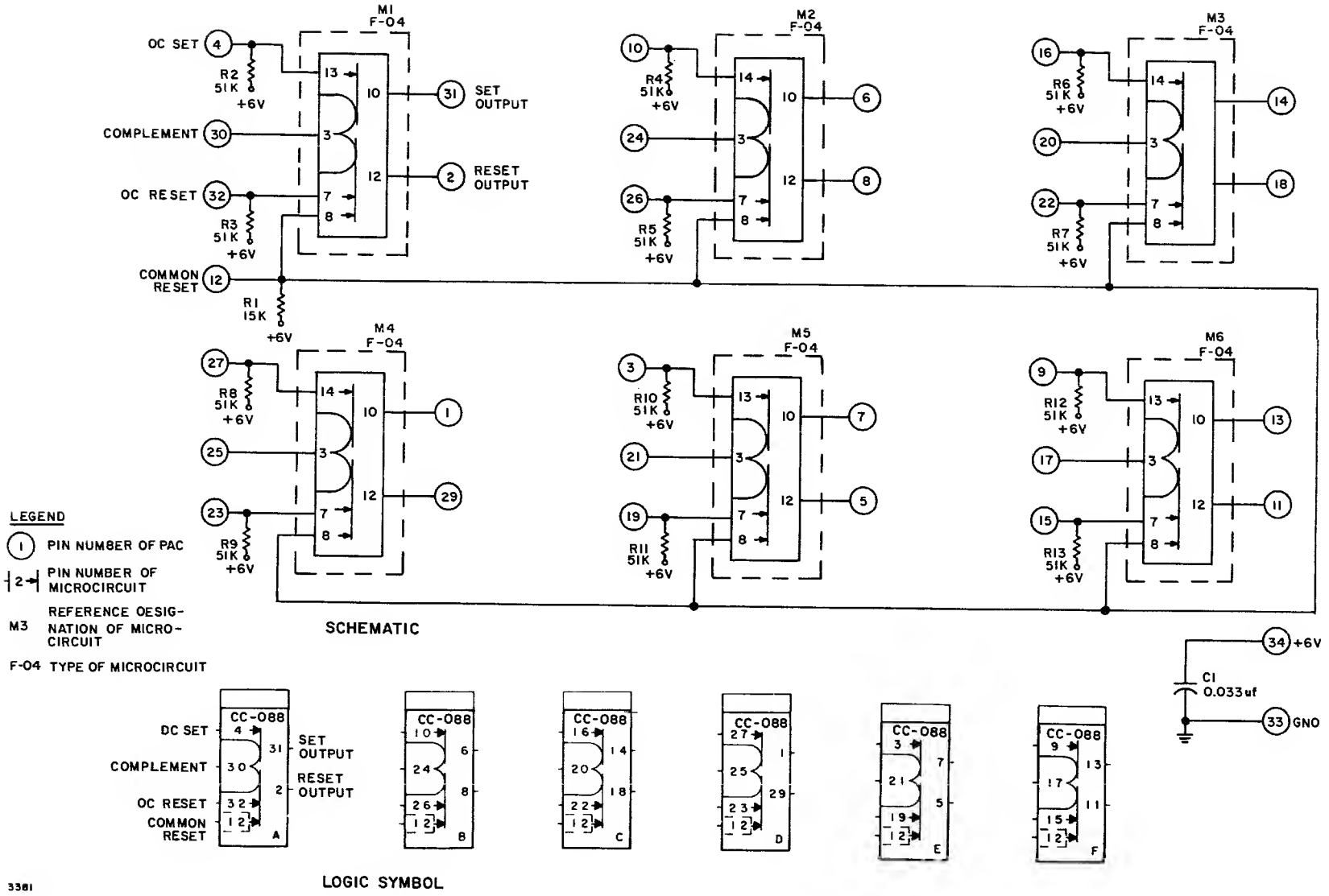
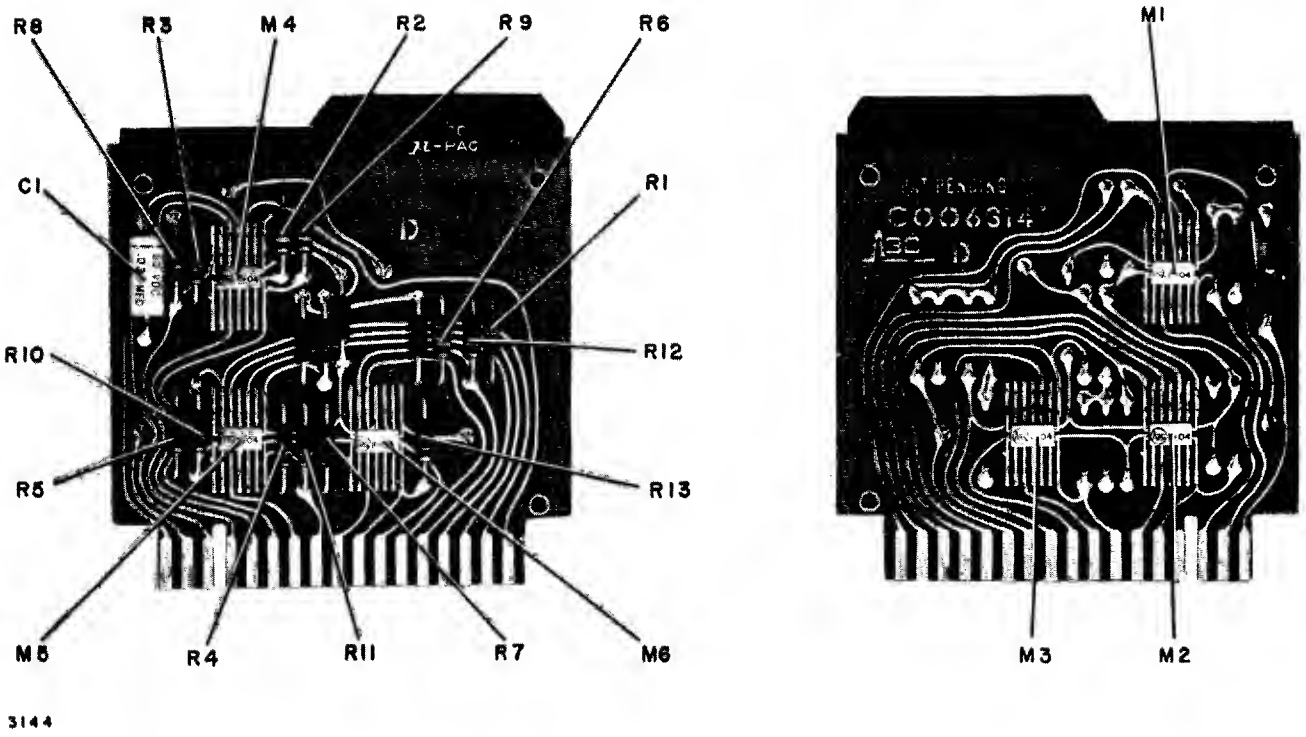


Figure A-47. Counter PAC, Model CC-088,
Schematic Diagram and Logic Symbol

Parts Location



Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1-M6	MICROCIRCUIT: F-04, flip-flop integrated circuit	950 100 004
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 µf ±20%, 50 vdc	930 313 016
R1	RESISTOR, FIXED, COMPOSITION: 15K ±5%, 1/4w	932 007 077
R2-R13	RESISTOR, FIXED, COMPOSITION: 51K ±5%, 1/4w	932 007 090

Figure A-48. Counter PAC, Model CC-088, Parts Location and Identification

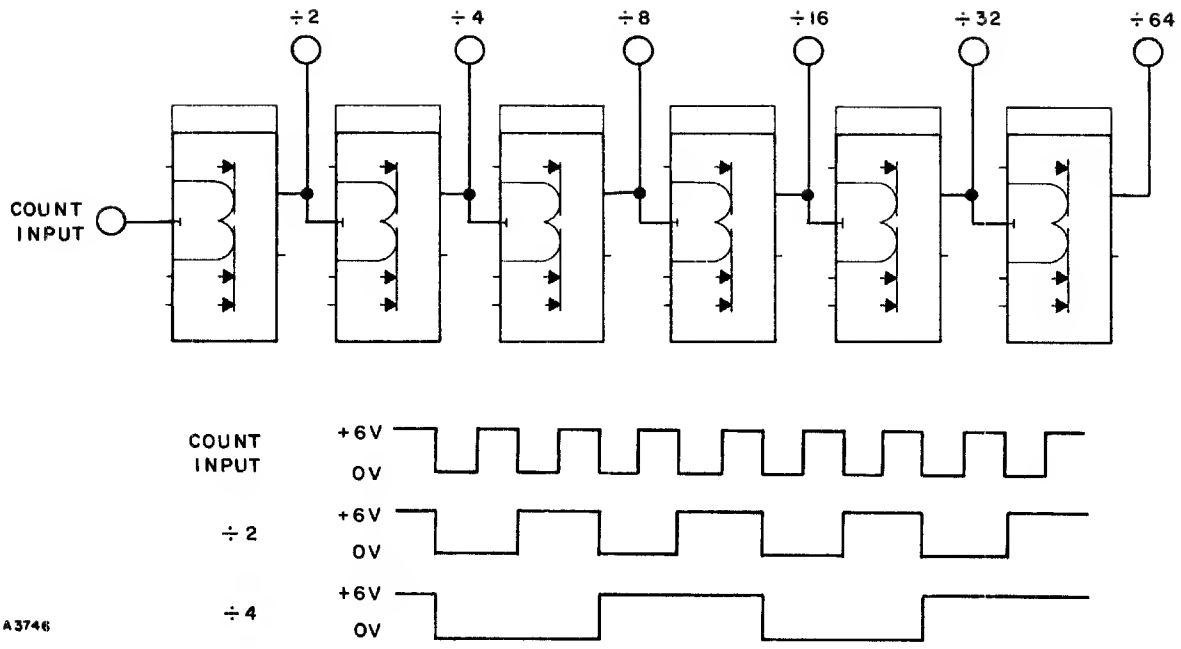


Figure A-49. Counter PAC, Model CC-088, Operation As a Frequency Divider

GATED FLIP-FLOP PAC, MODEL CC-089

The Gated Flip-Flop PAC, Model CC-089 (Figures 1 and 2), contains four independent flip-flops. A versatile input structure allows control from a variety of levels and pulses. Typical applications are storage, counting and shifting, and control.

INPUT AND OUTPUT SIGNALS

DC Set and DC Reset. -- A signal at 0v for 80 nsec or longer on a dc set (or reset) input will set (or reset) the flip-flop.

Common Reset. -- A signal at 0v for 80 nsec or longer on the common reset input clears all four stages simultaneously.

Set Control and Reset Control. --+6v is the enabling level on the control inputs.

Clock. -- The flip-flop changes state on the negative transition of the clock input.

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 mc

Input Loading

DC inputs:	2/3 unit load each
Control inputs:	1 unit load each
Common reset:	3 unit loads
Clock:	1 unit load each

Output Drive Capability

8 unit loads each

Circuit Delay

Clock input to set or reset output: 60 nsec (max)

DC set input to dc set output, or dc reset input to reset output: 80 nsec (max)

DC set input to reset output, or dc reset input to set output: 60 nsec (max)

Current Requirements

+6v: 100 ma (max)

Power Dissipation

0.60w (max)

Handle Color Code

Blue

APPLICATIONS

The CC-089 can be used as a counter (Figure 3) or as a shift register (Figure 4). The method of parallel information drop-in is shown in Figure 5.

Data may be transferred to the flip-flop with a single-ended signal by first resetting all stages, then setting the appropriate ones. For double-ended data transfer, complementary signals applied to the dc set and dc reset inputs set the flip-flop to the appropriate state in one operation.

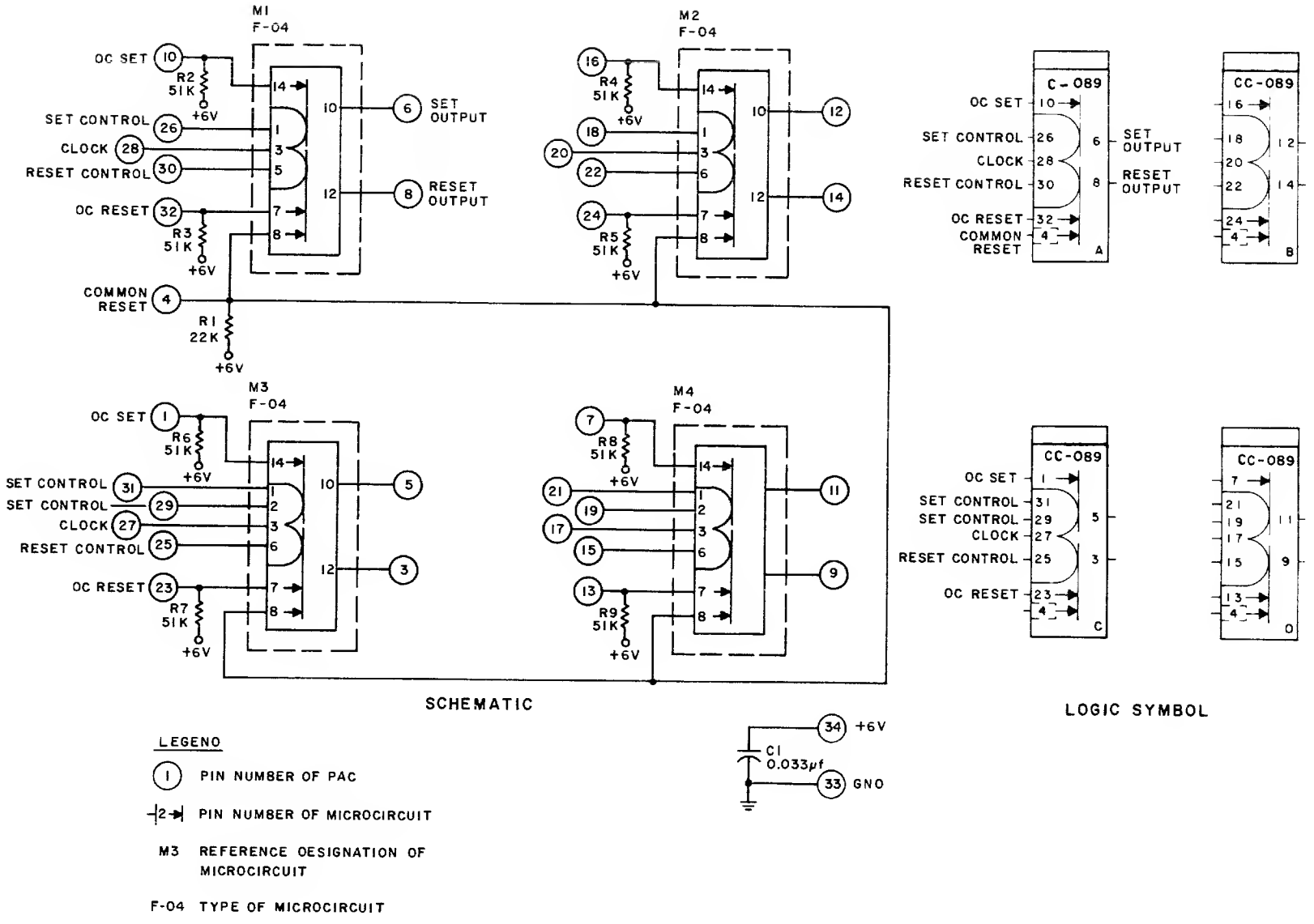
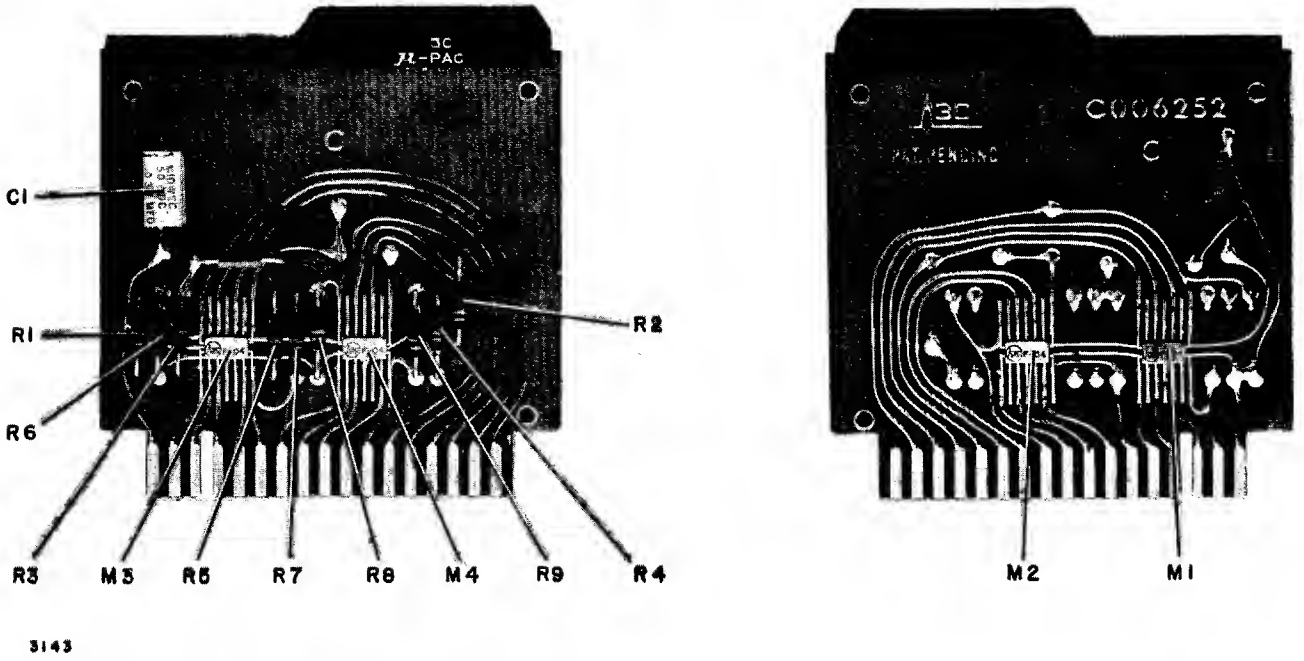


Figure 1. Gated Flip-Flop PAC, Model CC-089, Schematic Diagram and Logic Symbol

Parts Location



Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1-M4	MICROCIRCUIT: F-04, flip-flop integrated circuit	950 100 004
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
R1	RESISTOR, FIXED, COMPOSITION: 22K ±5%, 1/4w	932 007 081
R2-R9	RESISTOR, FIXED, COMPOSITION: 51K ±5%, 1/4w	932 007 090

Figure 2. Gated Flip-Flop PAC, Model CC-089, Parts Location and Identification

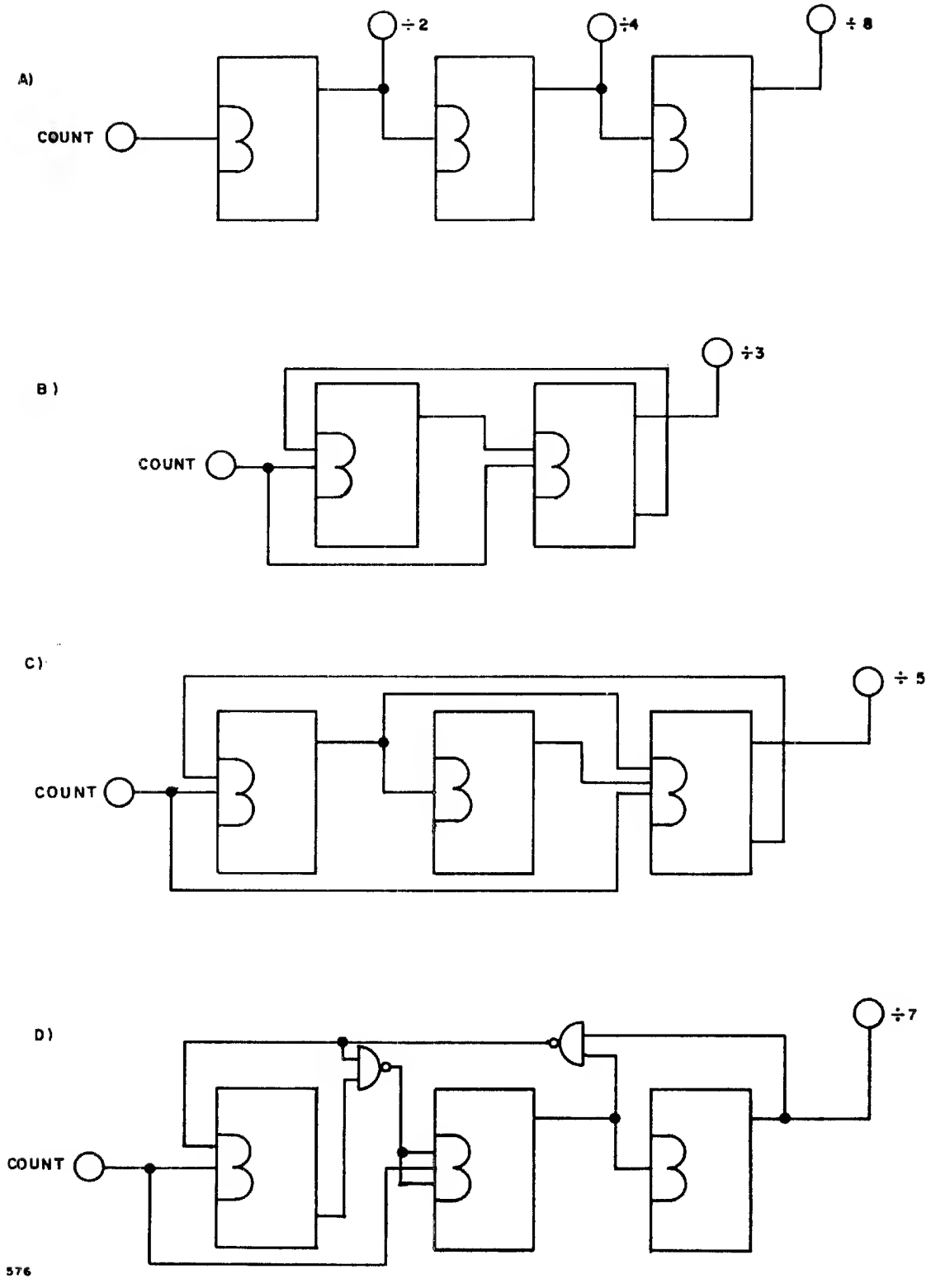


Figure 3. Gated Flip-Flop PAC, Model CC-089, Counter Operation

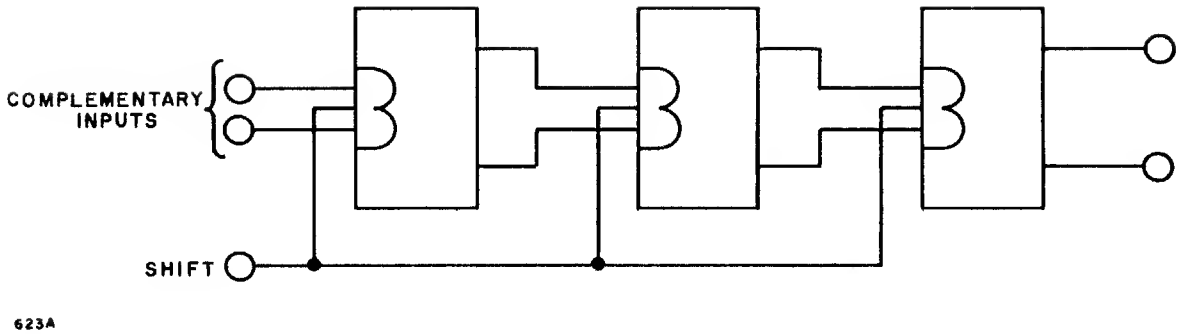


Figure 4. Gated Flip-Flop PAC, Model CC-089,
Shift Register Operation

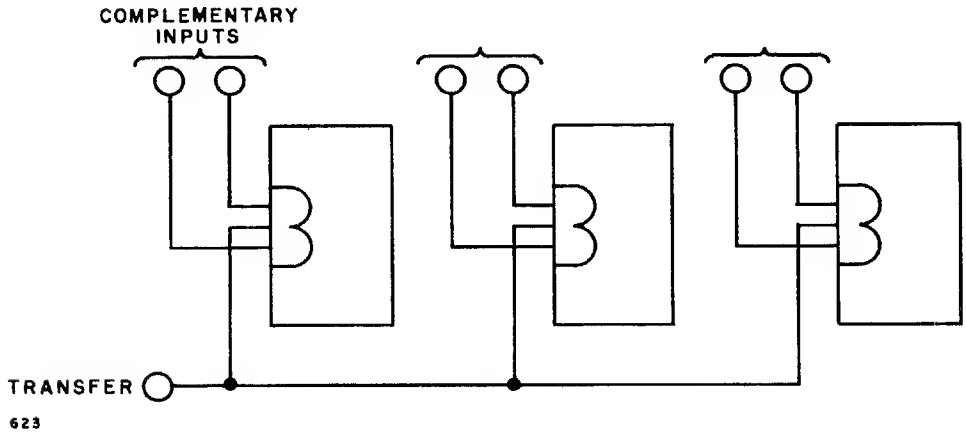


Figure 5. Gated Flip-Flop PAC, Model CC-089,
Parallel Information Drop-In

TERMINATION PAC, MODEL CC-090

GENERAL DESCRIPTION

The Termination PAC, Model CC-090 (Figure A-55), contains 32 resistors and 32 diodes which are used to clamp negative signals greater than -0.4v.

Electrical Parts List

Ref. Desig.	Description	3C Part No.
CR1-CR32	DIODE	943 024 001
R1-R32	RESISTOR, FIXED, COMPOSITION: 6.2 K ±5%, 1/4w	932 007 068

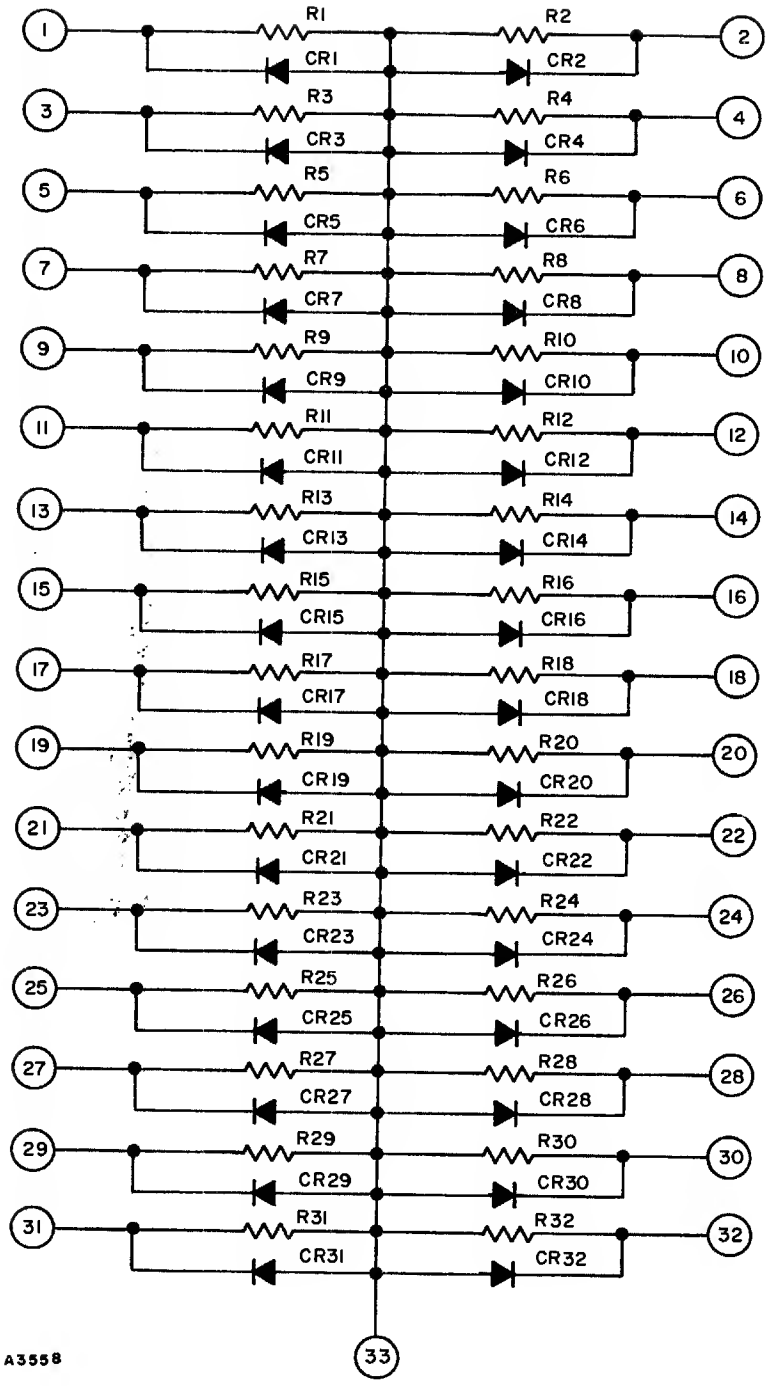


Figure A-55. Termination PAC, Model CC-090, Schematic Diagram

FAST CARRY COUNTER PAC, MODEL CC-091

The Fast Carry Counter PAC, Model CC-091 (Figures 1 and 2), contains eight pre-wired counter stages that can be set up by a few PAC connector jumpers to operate as an eight-stage binary counter or a two-digit BCD counter. In either configuration, carries are anticipated by gating structures, to reduce counter propagation delays.

Each stage has a dc set input for presetting a starting count, and a common reset input for clearing all eight stages simultaneously.

INPUT AND OUTPUT SIGNALS

Count. -- The contents of the counter increase by one on the negative transition of the count input. This input is the same as the clock input of the integrated circuit flip-flop.

Common Reset. -- A signal at 0v for 80 nsec or longer on the common reset input clears all eight counter stages simultaneously.

BCD and BIN inputs. -- These points are to be connected as shown in Figure 3 for binary counting or as shown in Figure 4 for BCD counting.

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 mc

Input Loading

DC set inputs: 2/3 unit load each
Common reset: 5 unit loads
Complement: 2 unit loads

Output Drive Capability

Output	Binary Mode	BCD Mode
A and E	5 unit loads each	5 unit loads each
$\overline{A}$ and $\overline{E}$	8 unit loads each	8 unit loads each
B and F	5 unit loads each	6 unit loads each
$\overline{B}$ and $\overline{F}$	8 unit loads each	8 unit loads each
C and G	6 unit loads each	7 unit loads each
$\overline{C}$ and $\overline{G}$	8 unit loads each	8 unit loads each
D	6 unit loads each	6 unit loads each
H	8 unit loads each	8 unit loads each
$\overline{D}$ and $\overline{H}$	8 unit loads each	6 unit loads each

Circuit Delay

Counter propagation delay per group of 4 stages:	100 nsec (max)
Counter propagation delay for the 8 stage counter:	200 nsec (max)
DC set input to set output, or common reset input to reset output:	80 nsec (max)
DC set input to reset output, or common reset input to set output:	60 nsec (max)

Current Requirements

+6v: 200 ma (max)

Power Dissipation

1.2w (max)

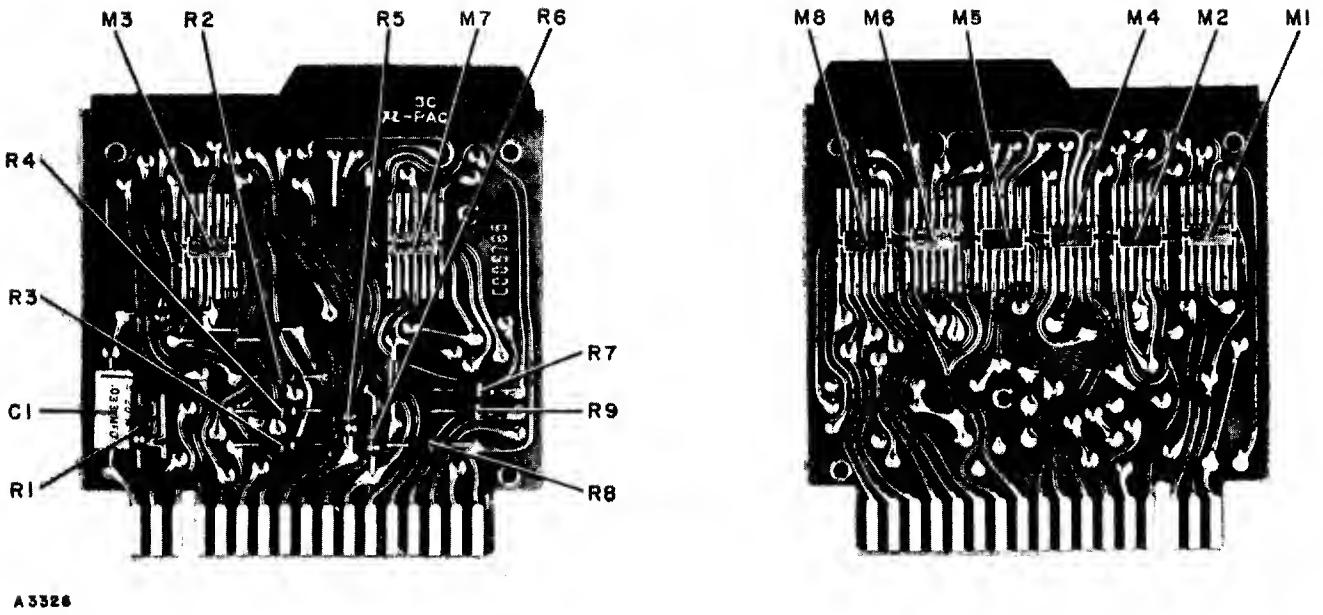
Handle Color Code

Blue

APPLICATIONS

Figure 3 shows the μ-PAC wired as an 8-bit binary counter. Frequency division by multiples of 2, up to 256, may be attained. Figure 4 shows the μ-PAC wired as a 2-decimal digit BCD counter. The counter can be preset to a number by first resetting all stages, then setting only the appropriate ones.

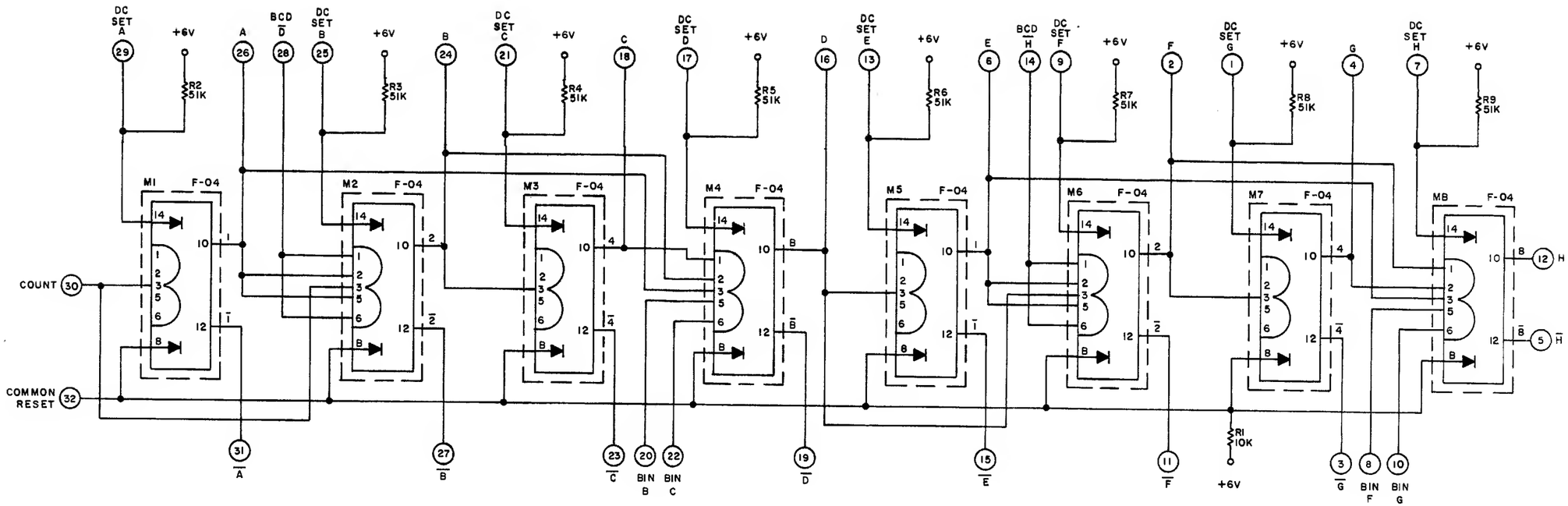
Parts Location



Electrical Parts List

Ref. Desig.	Description	Part No.
M1-M8	MICROCIRCUIT: F-04, flip-flop integrated circuit	950 100 004
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 µf ±20%, 50 vdc	930 313 016
R1	RESISTOR, FIXED, COMPOSITION: 10 K ±5%, 1/4w	932 007 073
R2-R9	RESISTOR, FIXED, COMPOSITION: 51 K ±5%, 1/4w	932 007 090

Figure 2. Fast Carry Counter PAC, Model CC-091, Parts Location and Identification



LEGEND

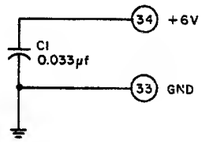
(1) PIN NUMBER OF PAC

2 PIN NUMBER OF MICROCIRCUIT

M3 REFERENCE DESIGNATION OF MICROCIRCUIT

F-04 TYPE OF MICROCIRCUIT

6224



SCHEMATIC

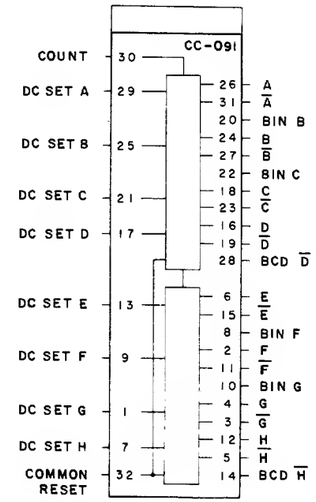


Figure 1. Fast Carry Counter PAC, Model CC-091, Schematic Diagram and Logic Symbol

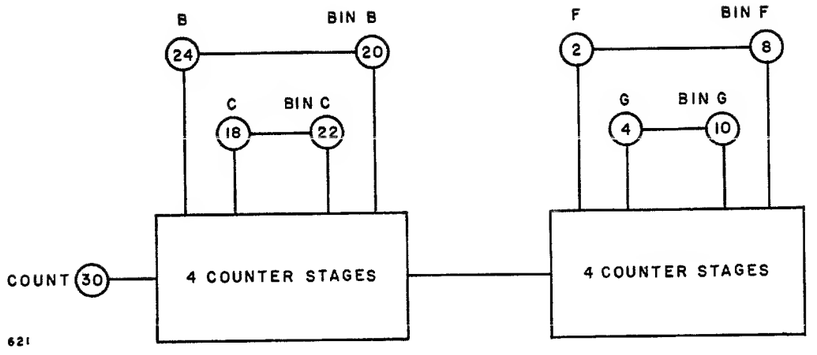


Figure 3. Fast Carry Counter PAC, Model CC-091, Jumper Connections for Binary Counting

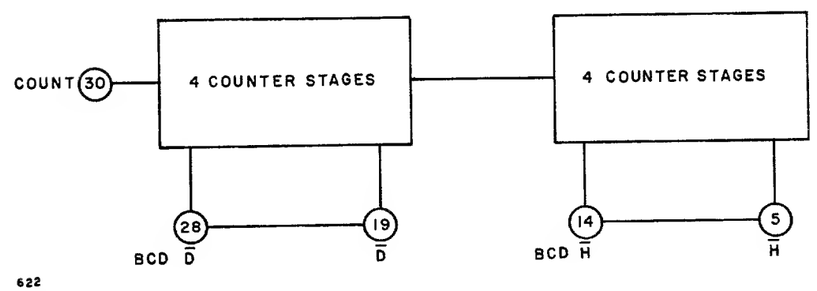


Figure 4. Fast Carry Counter PAC, Model CC-091, Jumper Connections for BDC Counting

BUFFER REGISTER PAC, MODEL CC-092

The Buffer Register PAC, Model CC-092 (Figures A-60 and A-61), contains six flip-flops. Common clock and common reset inputs make simultaneous operations possible on all stages. Typical uses include shifting, accumulating, and clocked parallel transfer.

INPUT AND OUTPUT SIGNALS

DC Set. -- A signal at 0v for 80 nsec or longer on dc set input will set the flip-flop.

Set Control and Reset Control. -- +6v is the enabling level on the control inputs.

Common Clock. -- The flip-flops change state on the negative transition of the clock input.

Common Reset. -- A signal at 0v for 80 nsec or longer on the common reset input clears all the six stages simultaneously.

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 mc

Input Loading

DC set:	2/3 unit load each
Control inputs:	1 unit load each
Common reset:	4 unit loads
Common clock:	6 unit loads

Output Drive Capability

8 unit loads each

Circuit Delay

Clock input to set or reset output: 60 nsec (max)

DC set input to set output, or common reset input to reset output: 80 nsec(max)

DC set input to reset output, or common reset input to set output: 60 nsec(max)

Current Requirements

+6v: 150 ma (max)

Power Dissipation

0.90w (max)

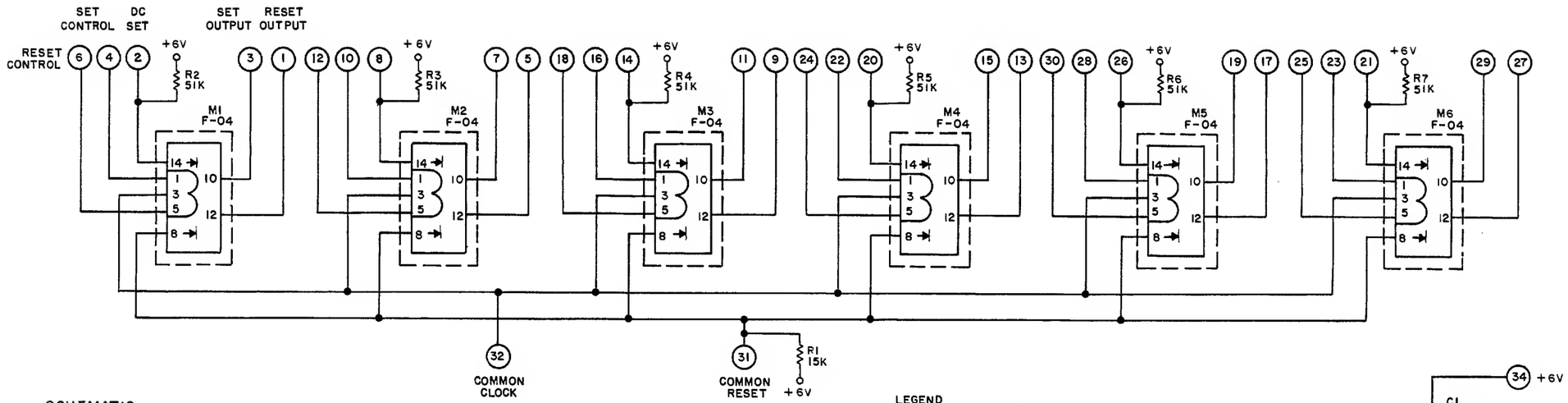
Handle Color Code

Blue

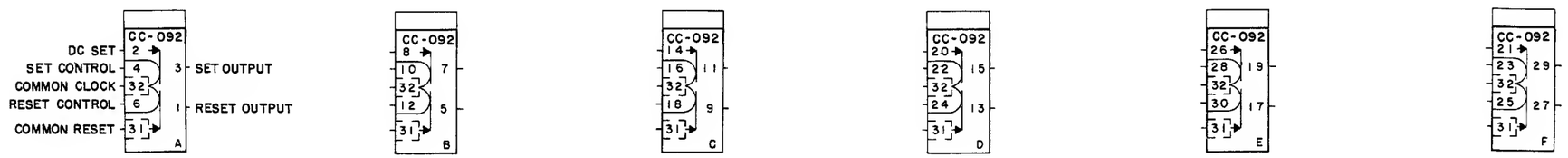
APPLICATIONS

The CC-092 can be used as a shift register in the configuration of Figure A-62. The method of parallel information drop-in is shown in Figure A-63.

For double-ended data transfer, complementary signals applied to the dc set and dc reset inputs set the flip-flop to the appropriate state in one operation. Data may be transferred to the flip-flop with a single-ended signal by first resetting all stages, then setting the appropriate ones.



SCHEMATIC

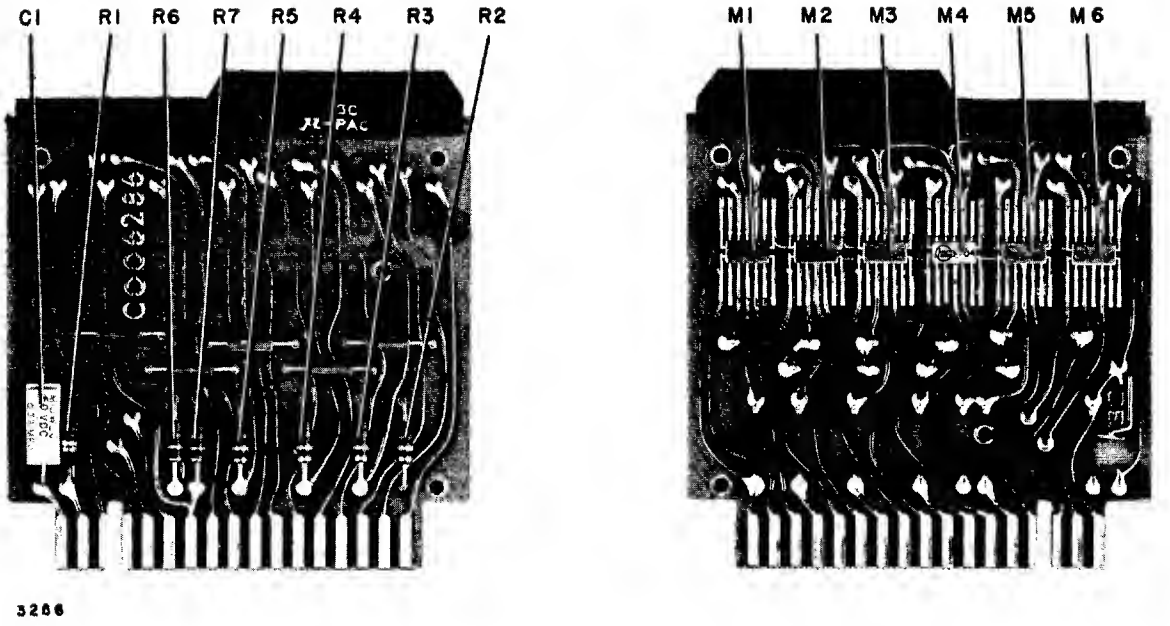


LOGIC SYMBOL

488A

Figure A-60. Buffer Register PAC, Model CC-092, Schematic Diagram and Logic Symbol

Parts Location



Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1-M6	MICROCIRCUIT: F-04, flip-flop integrated circuit	950 100 004
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
R1	RESISTOR, FIXED, COMPOSITION: 15K ±5%, 1/4w	932 007 077
R2-R7	RESISTOR, FIXED, COMPOSITION: 51K ±5%, 1/4w	932 007 090

Figure A-61. Buffer Register PAC, Model CC-092, Schematic Diagram and Logic Symbol

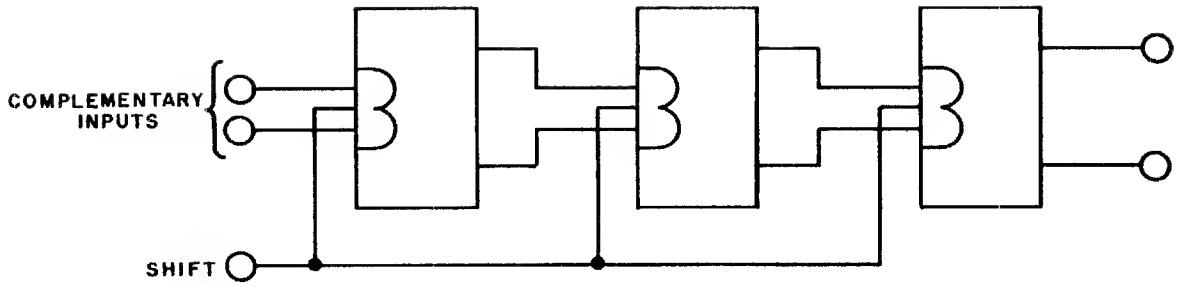


Figure A-62. Buffer Register PAC, Model CC-092, Shift Register Operation

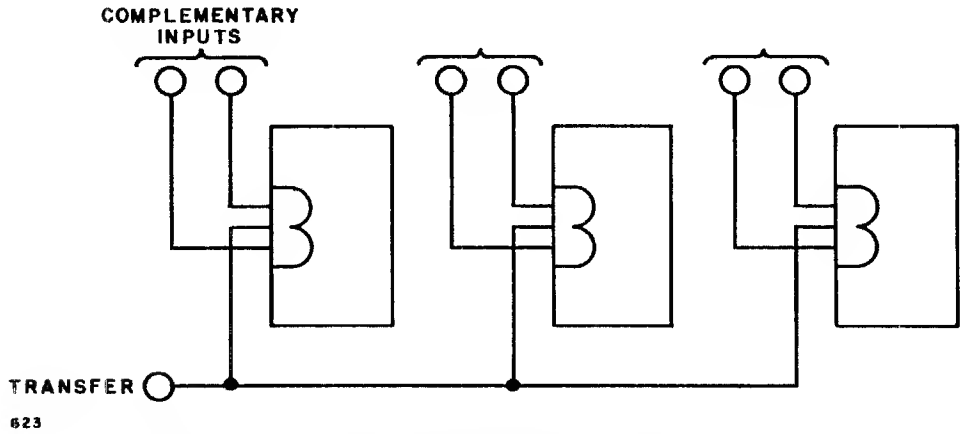


Figure A-63. Buffer Register PAC, Model CC-092, Parallel Information Drop-In

RESISTOR PAC, MODEL CC-130

The Resistor PAC, Model CC-130 (Figure A-58), consists of 20 1K resistors. One end of each resistor is brought out to a separate PAC pin. The other ends of the resistors are connected to $+V_{cc}$ on the PAC.

NOTE

The following pins must be jumpered together as indicated:

Pins 2 to 18 to 33
Pins 5 to 15 to 33

Electrical Parts List

Ref. Desig.	Description	3C Part No.
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 µf ±20%, 50 vdc	930 313 016
R1-R20	RESISTOR, FIXED, COMPOSITION: 1K ±5%, 1/4w	932 007 049

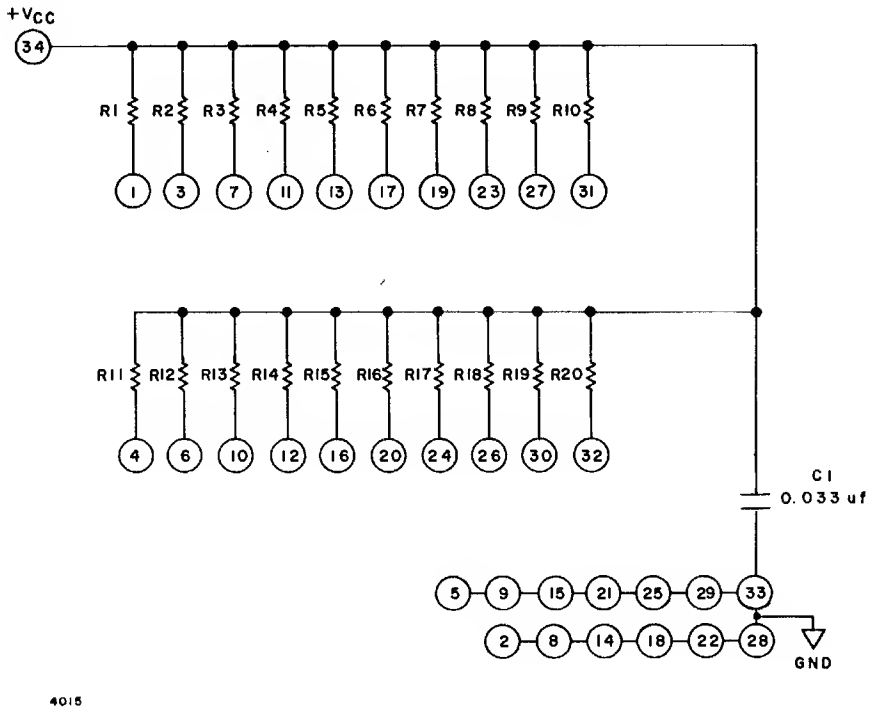


Figure A-63a. Resistor PAC, Model CC-130, Schematic Diagram

TRANSMISSION LINE DRIVER PAC, MODEL CC-153

The Transmission Line Driver PAC, Model CC-153 (Figure A-61), contains six identical circuits which drive twisted-pair cables at 1-mc repetition rates. The transmission line receivers should be a high impedance. A standard NAND gate is recommended.

The design principle is such that the PAC can drive up to 20 unit loads in a daisy chain without terminating resistors. The turn-on rise time is limited to a minimum of 35 nanoseconds by means of a Miller capacitor. Positive reflections due to line mismatch are clamped to ground at the receivers. The active pull-up on the output is short circuit protected by means of a series current limiting resistor which also serves as a partial series line-matching resistor.

CIRCUIT FUNCTION

Each driver circuit which performs a NAND function contains a 2-input F-02 amplifier microcircuit. Each circuit has a ground pin adjacent to the output terminals for the signal return from the transmission line.

SPECIFICATIONS

Frequency of Operation

DC to 5 mc

Input Loading

1 unit load each

Output Drive Capability

20 unit loads

Circuit Delay

60 nsec (typ)
80 nsec (max)

Output Waveform Characteristics

Rise time: 30 nsec (typ) positive voltage transition

Fall time: 40 nsec (typ) negative voltage transition

Current Requirements

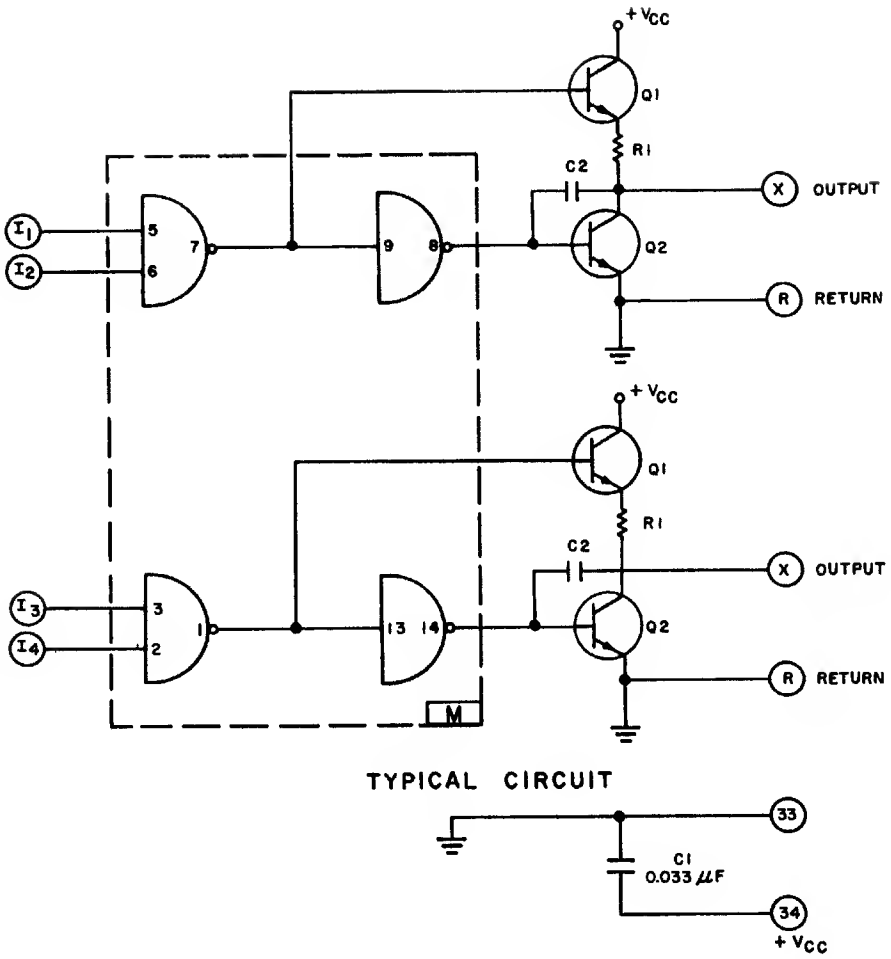
+6v: 120 ma (max)

Power Dissipation

0.8w (max)

Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1-M3	MICROCIRCUIT: F-02 quad NAND gate integrated circuit	950 100 002
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ± 20%, 50 vdc	930 313 016
C2	CAPACITOR, FIXED, CERAMIC DIELECTRIC: 33 pf ±10%, vdc	930 173 209
Q1, Q2	TRANSISTOR:	943 722 002
R1	RESISTOR, FIXED, COMPOSITION: 30 ohms ±5%, 1/4w	932 007 012



TYPICAL CIRCUIT

PIN DESIGNATIONS

CIRCUIT	I_1	I_2	I_3	I_4	M	X	R
A	—	—	20	22	3	19	25
B	28	30	—	—	3	27	21
C	—	—	26	12	2	15	13
D	16	18	—	—	2	7	9
E	—	—	14	6	1	3	4
F	8	10	—	—	1	2	1

LEGEND

(1) PIN NUMBER OF PAC

—|2 PIN NUMBER OF MICROCIRCUIT

M3 REFERENCE DESIGNATION OF MICROCIRCUIT

F-04 TYPE OF MICROCIRCUIT

A 4018

Figure A-63b. Transmission Line Driver PAC, Model CC-153, Schematic Diagram

TERMINATION PAC, MODEL CC-154

The Termination PAC, Model CC-154 (Figure A-62), contains 27 diode clamp circuits to prevent input signals from overshooting below ground. In addition, the PAC has eight inputs which have 1K resistors connected from input pins to +6 volts.

SPECIFICATIONS:

Frequency of Operation

5 mc

Input Loading

Inputs with resistors: 3 unit loads
Inputs without resistors: 0 unit loads

Current Requirements

+6v: 50 ma

Power Dissipation

300 mw (max.)

Electrical Parts List

Ref. Desig.	Description	3C Part No.
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 µf ±20%, 50 vdc	930 313 016
CR1-CR27	DIODE	943 024 002
R1-R8	RESISTOR, FIXED, COMPOSITION: 1K ±5%, 1/4w	932 007 049

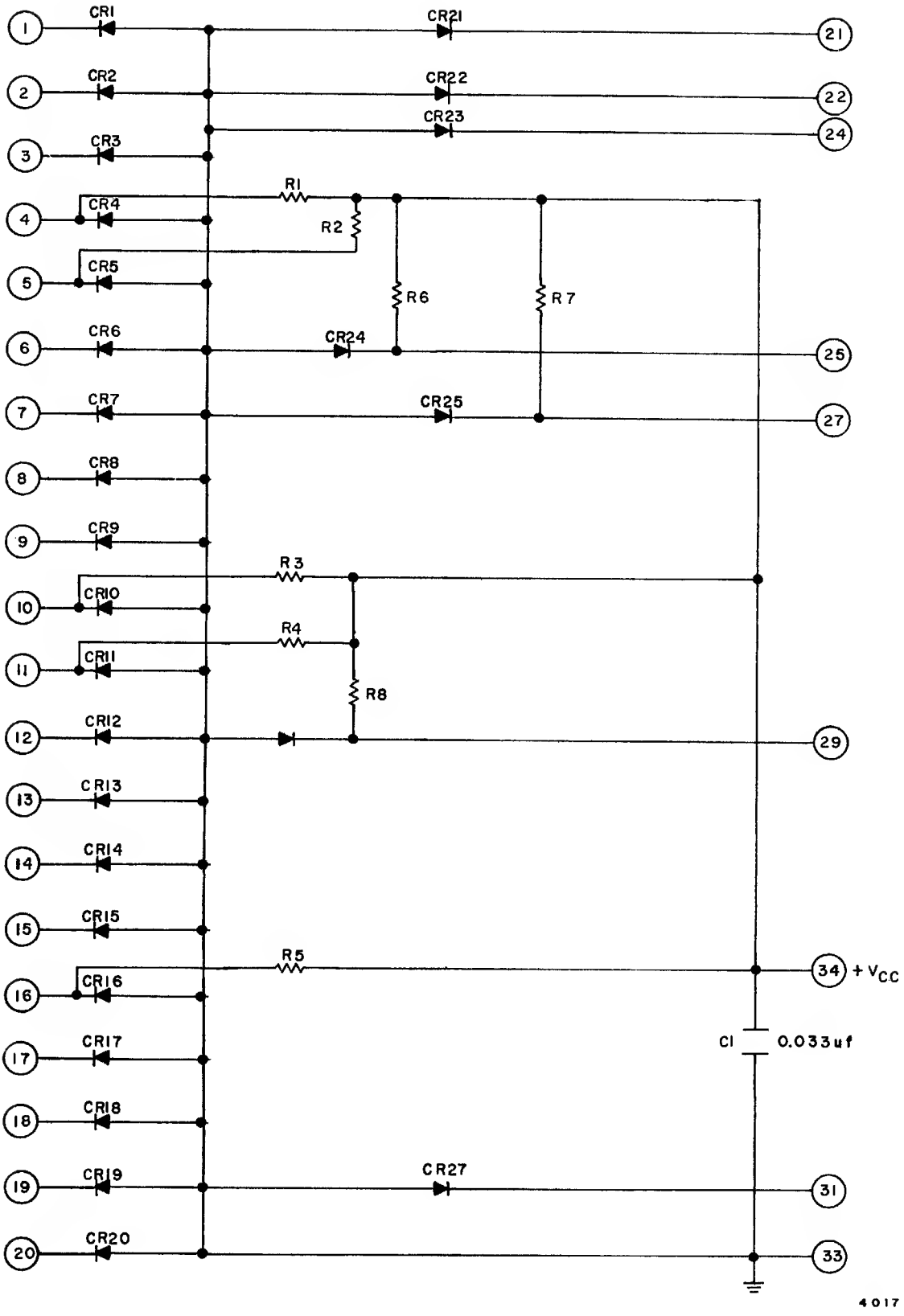


Figure A-63c. Termination PAC, Model CC-154, Schematic Diagram

TIMING DISTRIBUTOR PAC, MODEL CM-003

GENERAL DESCRIPTION

The timing Distributor PAC, Model CM-003 (Figure A-64 and A-65), provides accurately timed pulse sequences for use in timing and control applications. The CM-003 contains one control flip-flop, a 300-ns long delay line with 12 ns taps, a 50-ns long vernier delay line with 6 ns taps, and nine inverting power amplifier output circuits. Test points are shown in Figure A-66.

The PAC consists of two double-sided printed circuit boards sandwiched together for ease of mounting in a μ-BLOC. Board A, which plugs into the connector, contains the four delay lines (DL1 through DL4) and five F-03 microcircuit power amplifiers. The delay lines are positioned between the two circuit boards to expose the etched side of board A for timing jumper adjustment.

Board B contains an F-04 microcircuit flip-flop, discrete drivers, and termination loads.

NOTE

The CM-003 PAC occupies two slots in a taper-pin BLOC and three slots in a solderless-wrap BLOC, or the end slot (position 1) in either.

CIRCUIT FUNCTION

Delay lines DL1 through DL3 can be tapped and jumpered to the output power amplifiers and the vernier delay line, DL4, to provide accurately timed output pulses. Input connection points for each amplifier are located on the PAC to facilitate timing flexibility. Refer to Table A-1.

The dc reset of the flip-flop may also be tapped from any point along DL1 through DL3 to allow recirculation of the opposite driving edge, thereby establishing fixed pulse widths. An ac set, a dc reset, and the two outputs of the flip-flop are brought to the PAC connector.

Delay line DL4 and its associated output power amplifiers may be interconnected to provide pulses with a 6-ns delay resolution.

SPECIFICATIONS

Input Loading

Flip-flop dc reset: 2/3 unit load
Flip-flop ac set: 1 unit load
Power amplifiers: 2 unit loads each

Delay Line (DL1 through DL3)

Length: 300 ns ±5%, 24 taps, each 12.5 ±1 ns
Minimum pulse width: 85 ns
Maximum pulse width: 330 ns

Circuit Delay

Flip-flop:

Set input to set output or reset input to reset output

65 ns (typ); 80 ns (max)

Set input to reset output or reset input to set output

45 ns (typ); 60 ns (max)

Power amplifiers:

24 ns (typ); 30 ns (max) each

Delay to first tap (C1):

60 ns (typ); 80 ns (max)

Output Drive Capability

Flip-flop set:	8 unit loads
Flip-flop reset:	4 unit loads
Power amplifers:	25 unit loads each

Vernier Delay Line (DL4)

Length:

50 ns ±5%, 8 taps, each 6 ±1 ns

Current Requirements

+6v:	175 ma
-6v:	4 ma

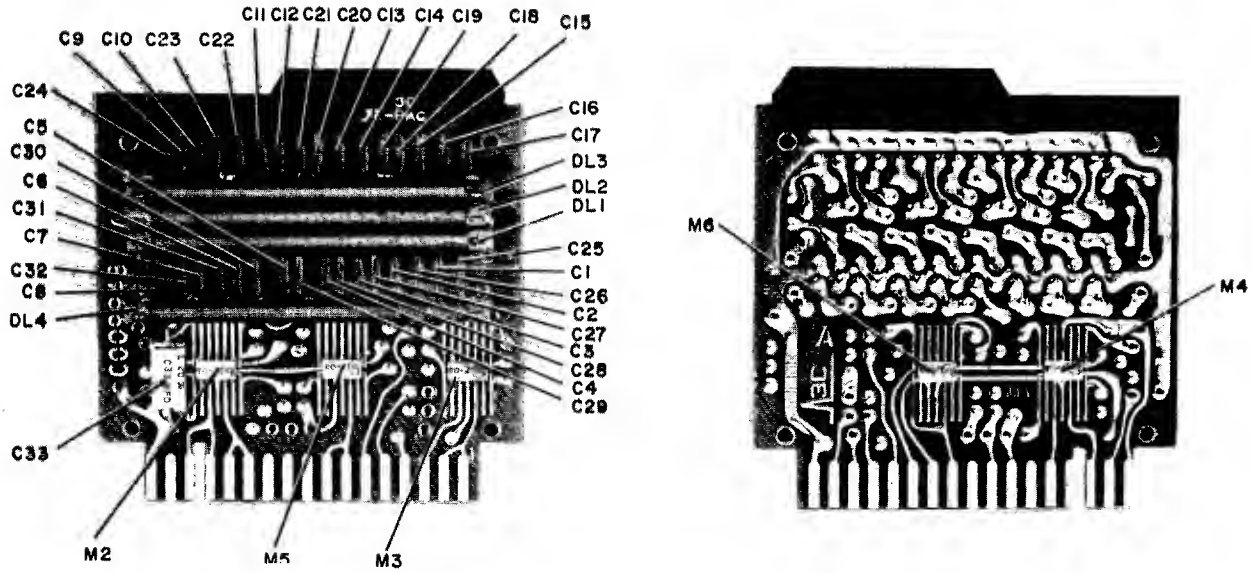
Power Dissipation

1.10w (max)

NOTE

This document contains the information stated in Revision A of 3C Document No. B010797.

Board A



Board B

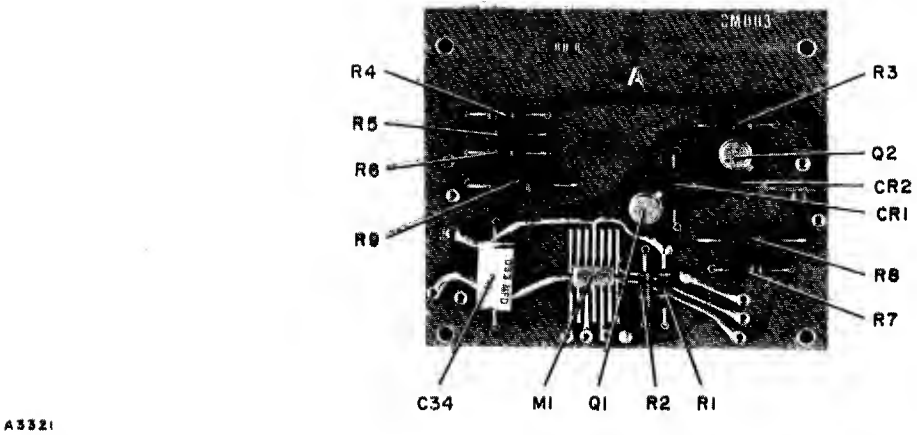
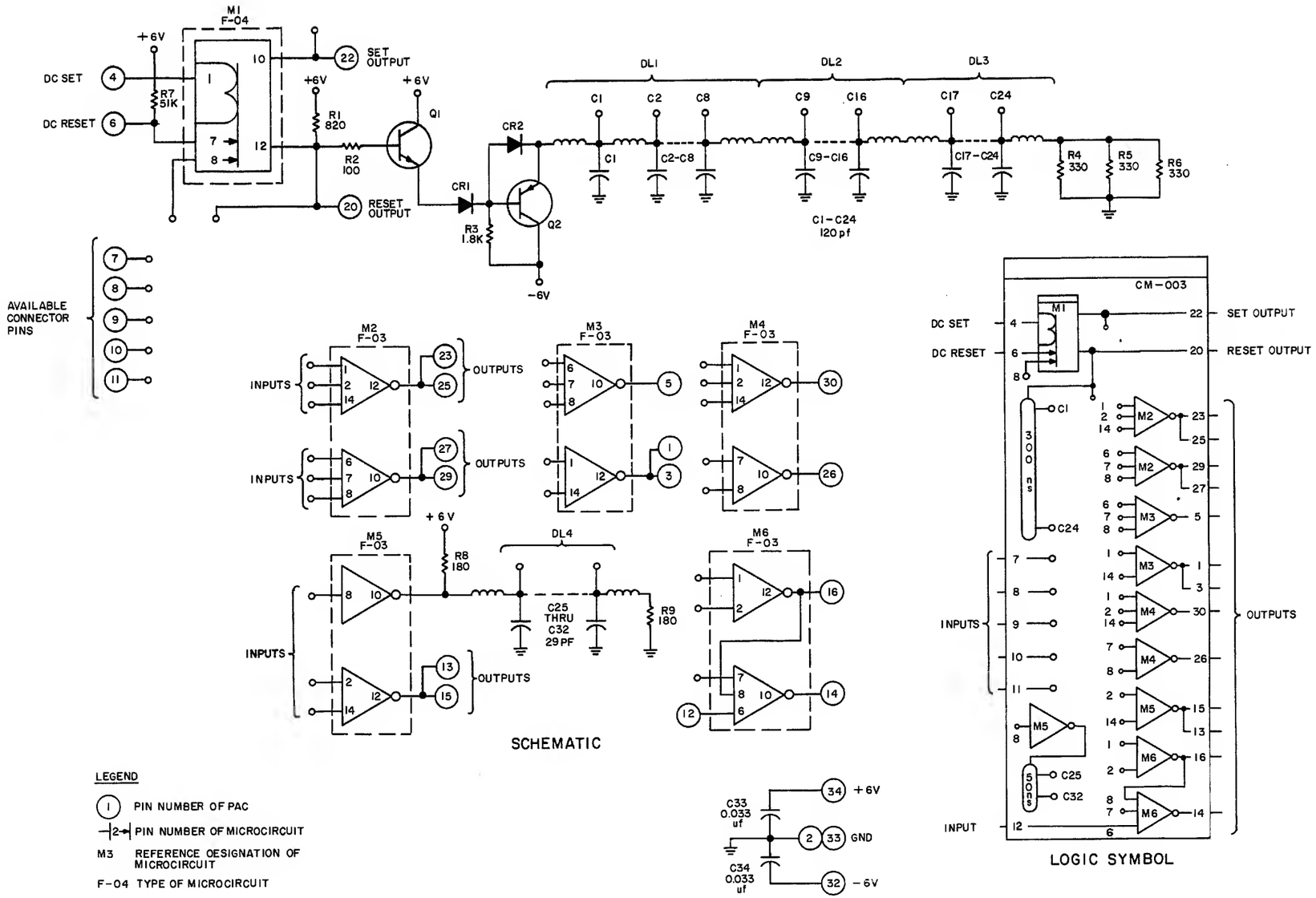


Figure A-64. Timing Distributor PAC, Model CM-003, Parts Location and Identification (Sheet 1 of 2)

Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1	MICROCIRCUIT: F-04, flip-flop integrated circuit	950 100 004
M2-M6	MICROCIRCUIT: F-03, power amplifier integrated circuit	950 100 003
C1-C24	CAPACITOR, FIXED, MICA DIELECTRIC: 120 pf ±2%, 100 vdc	930 004 219
C25-C32	CAPACITOR, FIXED, MICA DIELECTRIC: 29 pf ±2%, 100 vdc	930 004 204
C33, C34	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
CR1, CR2	DIODE:	943 088 001
DL1-DL4	COIL, DELAY LINE:	
Q1	TRANSISTOR: Replacement Type 2N3011	943 722 001
Q2	TRANSISTOR: Replacement Type 2N3012	943 721 001
R1	RESISTOR, FIXED, COMPOSITION: 820 ohms ±5%, 1/4w	932 007 047
R2	RESISTOR, FIXED, COMPOSITION: 100 ohms ±5%, 1/4w	932 007 025
R3	RESISTOR, FIXED, COMPOSITION: 1.8K ±5%, 1/4w	932 007 055
R4-R6	RESISTOR, FIXED, COMPOSITION: 330 ohms ±5%, 1/4w	932 007 037
R7	RESISTOR, FIXED, COMPOSITION: 51K ±5%, 1/4w	932 007 090
R8, R9	RESISTOR, FIXED, COMPOSITION: 180 ohms ±5%, 1/2w	932 004 031

Figure A-64. Timing Distributor PAC, Model CM-003, Parts Location and Identification (Sheet 2 of 2)



NOTES

TAP DESIGNATIONS REFER TO CIRCUIT COMPONENTS. EXAMPLE: C1 TO TAP AT C1; 3-8 TO TAP AT M-3, PIN 8, 10 TO TAP AT PIN 10 OF PAC.

REFER TO TABLE I FOR DELAY LINE DELAYS IN NANOSECONDS.

B 3121

LEGEND

(1) PIN NUMBER OF PAC

—|2→| PIN NUMBER OF MICROCIRCUIT

M3 REFERENCE DESIGNATION OF MICROCIRCUIT

F-04 TYPE OF MICROCIRCUIT

Figure A-65. Timing Distributor PAC, Model CM-003, Jumper Interconnection Diagram, Schematic Diagram, and Logic Symbol

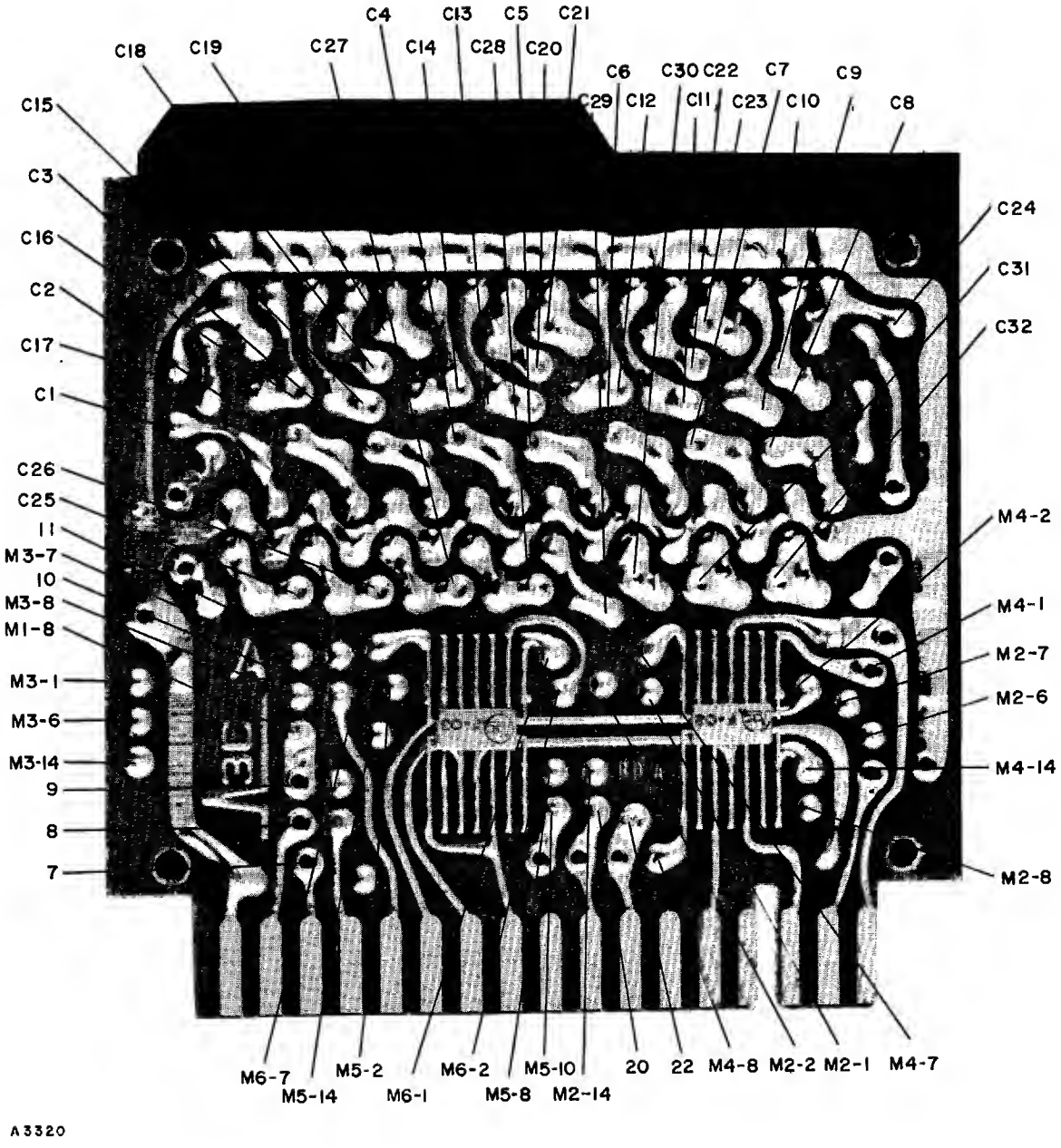


Figure A-66. Timing Distributor PAC, Model CM-003, Test Points

Table A-1.
Delay Line Tap Points with Corresponding Delay Line Delays
(Refer to Figure A-65)

Delay Line Jumper Connection	Delay Line Delay (ns)	Delay Line Jumper Connection	Delay Line Delay (ns)
C1	12	C19	228
C2	24	C20	240
C3	36	C21	252
C4	48	C22	264
C5	60	C23	276
C6	72	C24	288
C7	84		
C8	96		
C9	108		
C10	120		
C11	132	C25	6
C12	144	C26	12
C13	156	C27	18
C14	168	C28	24
C15	180	C29	30
C16	192	C30	36
C17	204	C31	42
C18	216	C32	48

SELECTION PAC, MODEL CM-006/106

GENERAL DESCRIPTION

The Selection PAC, Model CM-006/106 (Figures A-67 and A-68), contains eight transformer driven transistor switches connected as four (read-write) switch pairs. The CM-006 utilizes two F-03 microcircuit power amplifiers with decoding inputs for two address bits and a decoding enable input. An F-06 microcircuit multi-emitter gate provides timing (read-write) and matrix enable inputs. The PAC may be used as an 'X' pr 'Y' selection switch or sink.

The CM-106 PAC does not contain the F-03 integrated circuits for address input decoding but is otherwise similar to the CM-006.

CIRCUIT FUNCTION

Two binary address inputs are decoded to select one of the four F-03 integrated circuits. When the decoding enable input is passive, the output of the selected F-03 circuit will be at 0v. The multi-emitter circuit is turned on when the timing and matrix enable inputs are at +6v. Current flows through the primary of the transformer which is connected to the enabled F-03 and F-06 circuits. The output transistor is turned on by the secondary of the selected transformer.

The basic selection scheme of the CM-006 can be expanded by jumpering pins 3, 5, 9, and 24 to the corresponding pins on the CM-106. Decoding of the two address inputs will then be common to both PACs. Further expansion is possible by using the common F-03 and F-06 circuit inputs.

SPECIFICATIONS

Input Loading

Timing (read-write) inputs:	1 unit load
Matrix enable inputs:	2 unit loads
Address inputs:	3 unit loads
Decoding enable inputs:	4 unit loads

Outputs Characteristics

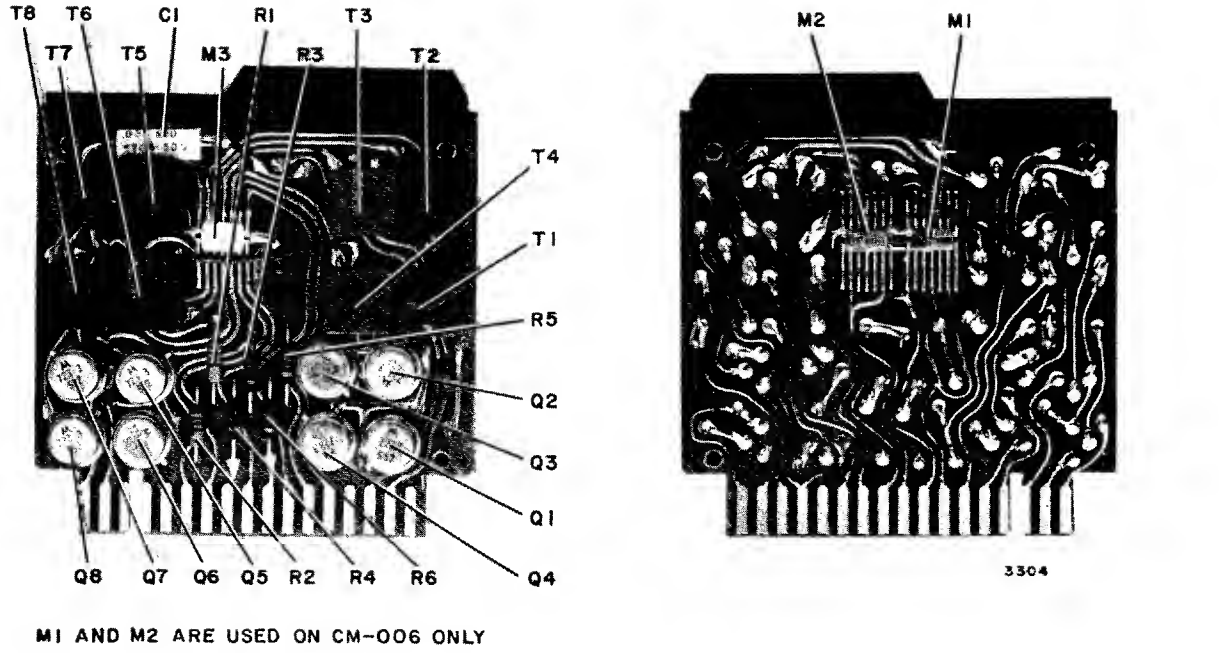
Turn-on delay (1.5v of timing input to 10% of output current):	40 ns (max)
Turn-off delay (1.5v of decoding enable input to 90% of output current):	90 ns (max)
Rise time (10%-90%):	80 ns (max)
Fall time (90%-10%):	80 ns (max)
Current:	425 ma (max)
Voltage:	30v (max)
Pulse width:	400 ns (max)
Duty cycle:	45% (max)

Current Requirements	Power Dissipation (400 ma output current)
CM-006: +6 100 ma (max)	CM-006: 1.5w (max)
CM-106: +6 65 ma (max)	CM-106: 1.3w (max)

NOTE

This document contains the information stated in Revision B of 3C Document No. B011157.

Parts Location

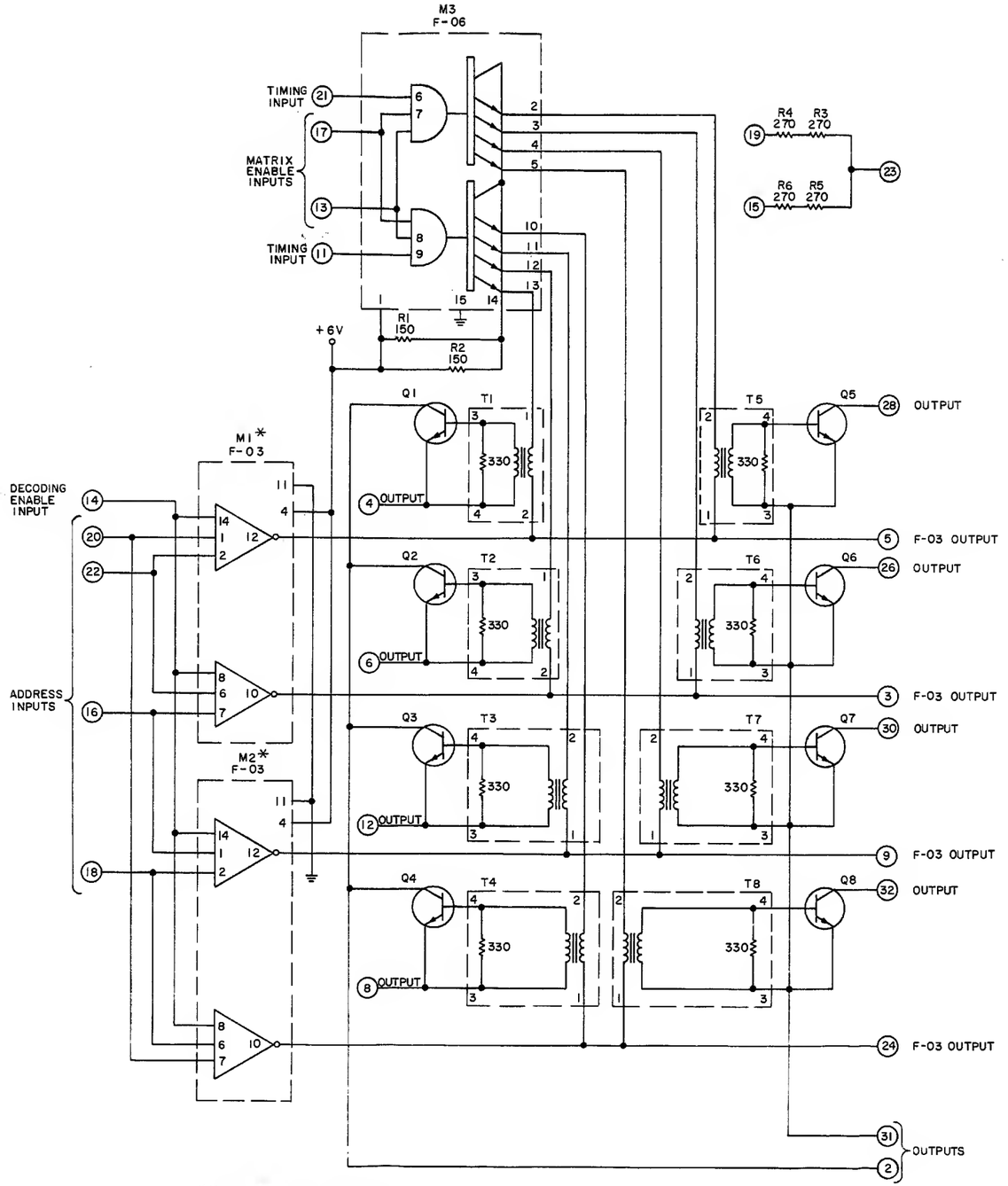


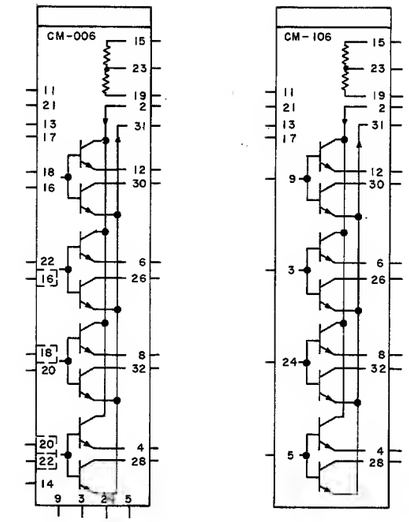
M1 AND M2 ARE USED ON CM-006 ONLY

Electrical Parts List

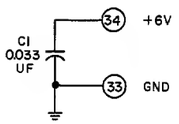
Ref. Desig.	Description	3C Part No.
M1, M2	MICROCIRCUIT: F-03, power amplifier integrated circuit	950 100 003
M3	MICROCIRCUIT: F-06, multi-emitter integrated circuit	950 100 006
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 µf ±20%, 50 vdc	930 313 016
Q1-Q8	TRANSISTOR:	943 723 003
R1, R2	RESISTOR, FIXED, FILM: 150 ohms ±2%, 1/4w	932 114 029
R3-R6	RESISTOR, FIXED, COMPOSITION: 270 ohms ±5%, 1/4w	932 007 035
T1-T8	TRANSFORMER, PULSE:	938 018 001

Figure A-67. Selection PAC, Model CM-006/106, Parts Location and Identification





LOGIC SYMBOL



LEGEND

(1) PIN NUMBER OF PAC

—|2|— PIN NUMBER OF MICROCIRCUIT

M3 REFERENCE DESIGNATION OF MICROCIRCUIT

F-04 TYPE OF MICROCIRCUIT

Figure A-68. Selection PAC, Model CM-006/106, Schematic Diagram and Logic Symbol

PARALLEL TRANSFER GATE PAC, MODEL CM-022

GENERAL DESCRIPTION

The Parallel Transfer Gate PAC, Model CM-022 (Figure A-69), utilizes seven F-01 dual NAND gate microcircuits containing fourteen 2-input NAND gates without collector resistors. These circuits provide a facility for connecting the NAND gates in parallel without decreasing the output drive capability.

The PAC can be used for the common transfer control of up to fourteen data signals. The data when transferred is inverted in polarity.

CIRCUIT FUNCTION

The NAND gates are arranged in four independent groups. Two of the groups contain four NAND gates each, one input being common to the four gates. The remaining two groups contain three NAND gates each, one input being common to the three gates.

Each gate performs the NAND function with conventional positive logic (+6v = ONE, 0v = ZERO). When both inputs are at passive or open, the output transistor is turned on, and the output is active (ground). If any input is at ground, the transistor is turned off, and the output is passive (the supply voltage, +6v).

The four common inputs can be externally connected to transfer a maximum of 14 bits of data simultaneously. With this arrangement, the data to be transferred is connected to the individual input of each gate and a strobe input is applied to the common input.

SPECIFICATIONS

Frequency of Operation

DC to 5 mc

Input Loading

Individual inputs:
1 unit load each

Common inputs:
1 unit load per gate

Output Drive Capability

8 unit loads

Circuit Delay (measured at +1.5v averaged over two stages)

30 ns (max)

Current Requirements

+6v: 95 ma (max)

Power Dissipation

560 mw (max)

Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1 - M7	MICROCIRCUIT: F-01, dual NAND gate integrated circuit	950 100 001
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016

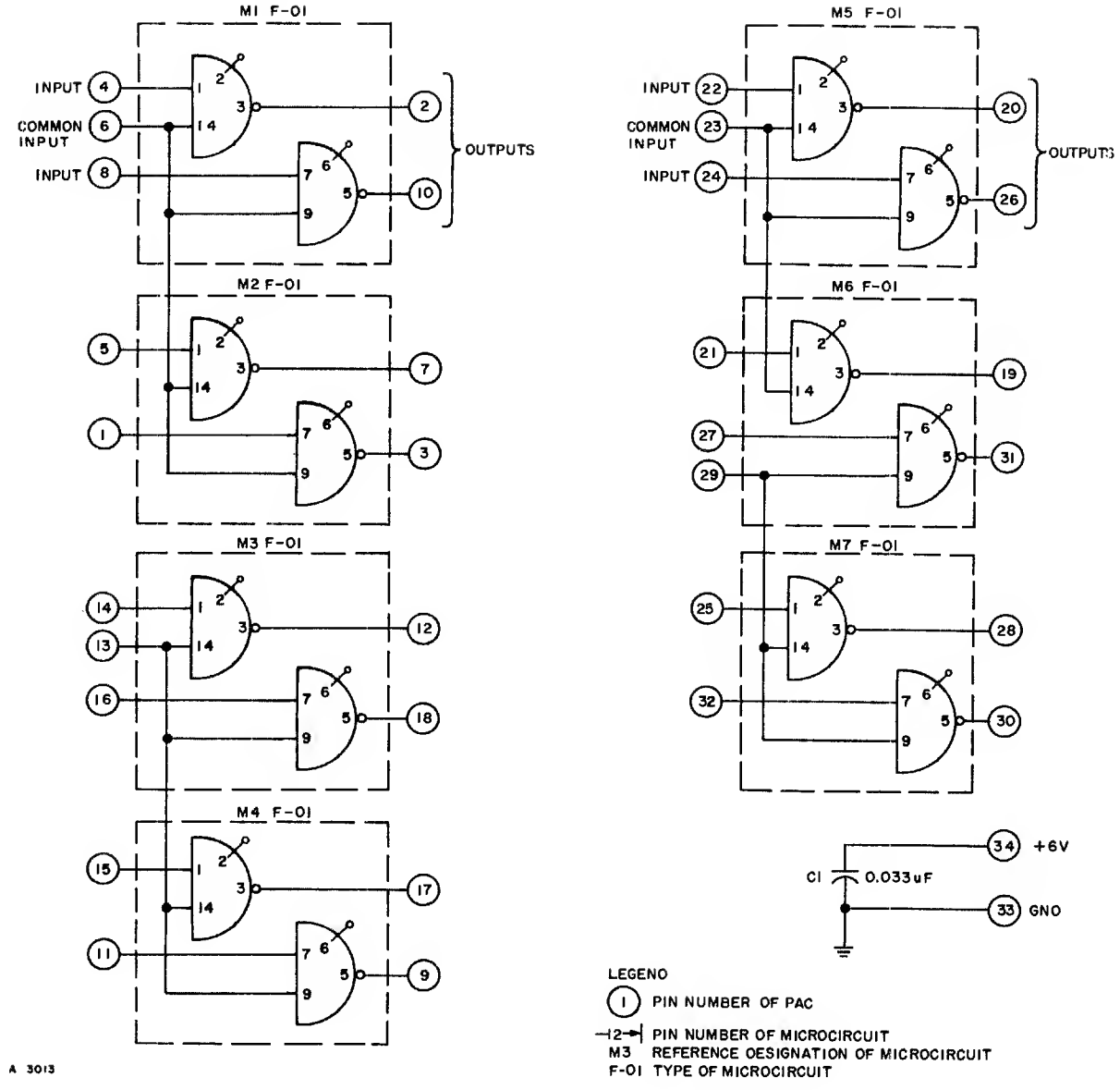


Figure A-69. Parallel Transfer Gate PAC, Model CM-022, Schematic Diagram

SENSE AMPLIFIER PAC, MODEL CM-032

The Sense Amplifier PAC, Model CM-032 (Figure A-70), contains four sense amplifier channels which amplify the core outputs on memory sense lines and convert the information content to μ-PAC logic levels. Inputs to each of the channels are differential signals on twisted pair lines. These information signals are measured differentially across pins 1 and 3, 7 and 8, 9 and 11, and 14 and 15 and are approximately 50 mv in amplitude.

A strobe input is provided which, when grounded, disables the sense amplifier channels. Strobe enable inputs are provided to gate the strobe input pairs of sense amplifier channels. An amplifier will be enabled when both the strobe and strobe enable inputs are asserted at that amplifier.

In addition to the direct outputs on each sense amplifier channel, outputs with series 62-ohm terminations are provided on two of the channels. The sense amplifier input ground return is generally connected to logic ground.

SPECIFICATIONS

Current Requirements

+6v: 120 ma
-6v: 80 ma
Strobe input at ground

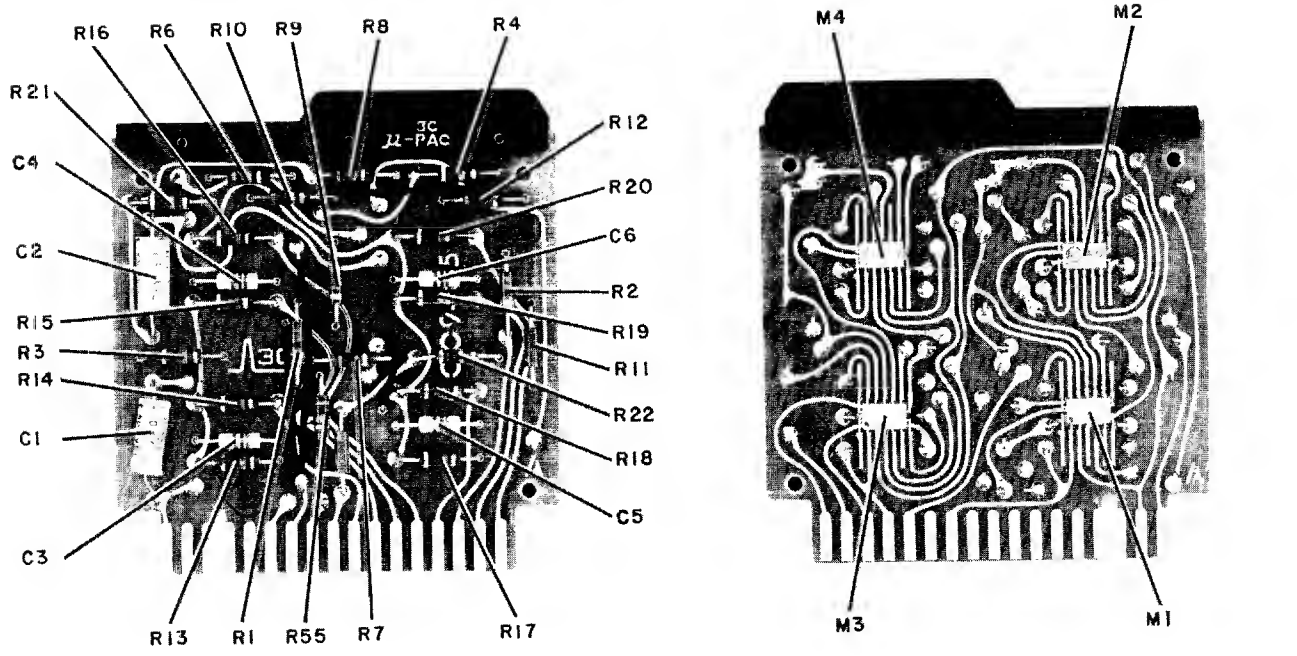
Threshold

Min. one signal: 45 mv

Max. zero signal: 25 mv

Circuit Delay

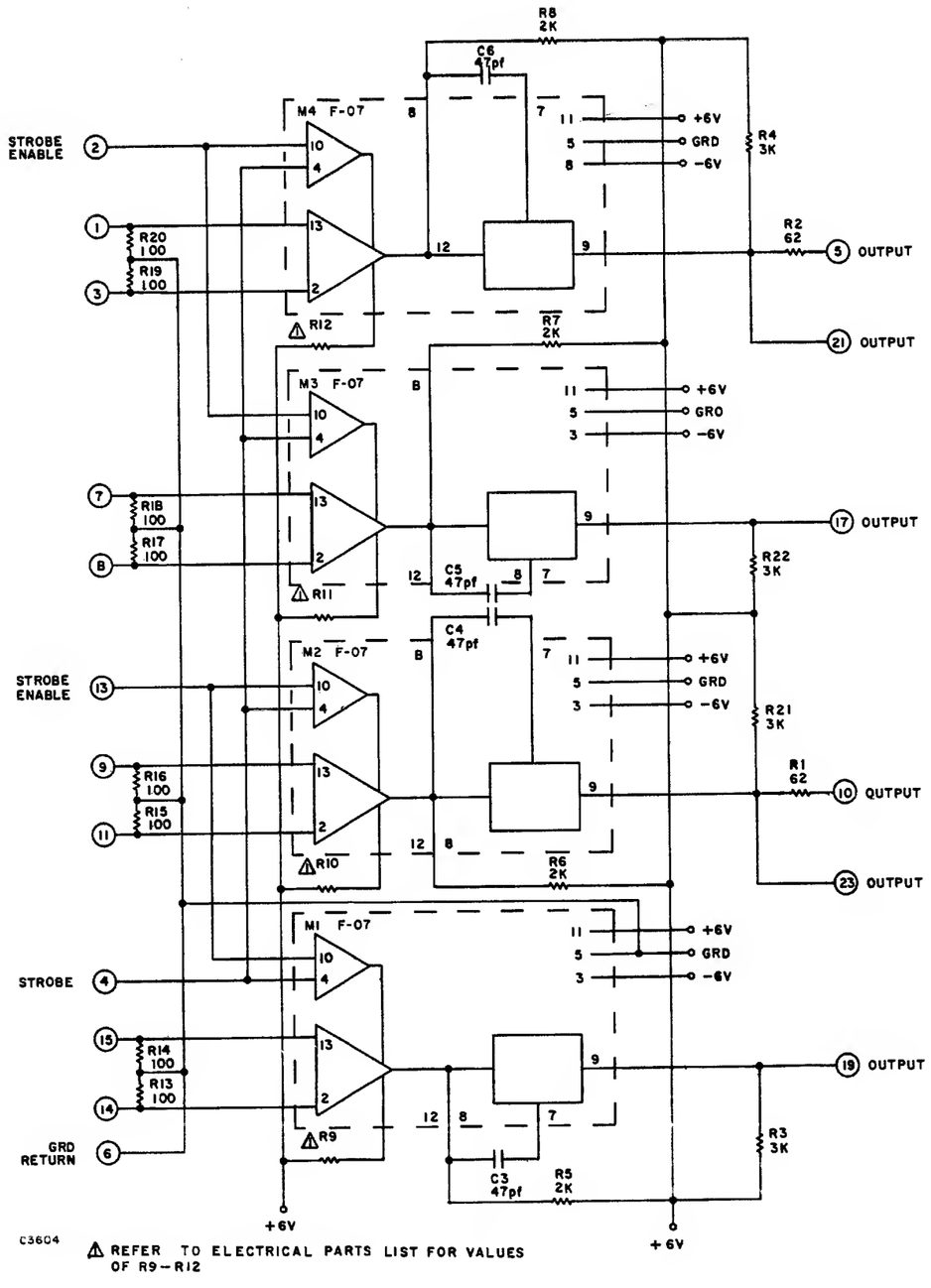
Strobe input (Pin 4) to output (Pins 17 and 19): 30 ±15 nsec

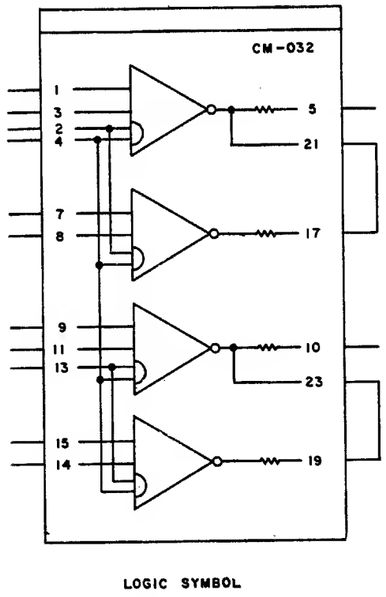


6789 Figure A-70. Sense Amplifier PAC, Model CM-032, Parts Location

Electrical Parts List (A013799J)

Ref. Desig.	Description	Part No.
M1-M4	MICROCIRCUIT: F-07, Sense Amplifier Integrated Circuit	950 100 007
C1-C2	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 µf ±20%, 50 vdc	930 313 016
C3-C6	CAPACITOR, FIXED, CERAMIC DIELECTRIC: 47 pf ±5%, 100 vdc	930 173 111
R1-R2	RESISTOR, FIXED, COMPOSITION: 62 ohms ±5%, 1/4 w	932 007 020
R3, R4, R21, R22	RESISTOR, FIXED, COMPOSITION: 3K ±2%, 1/4 w	932 114 060
R5-R8	RESISTOR, FIXED, COMPOSITION: 2K ±2%, 1/4 w	932 114 056
R9-R12	RESISTOR, FIXED, COMPOSITION: 75 ohms ±2%, 1/4 w, F-07 color dot - violet 120 ohms ±2%, 1/4 w, F-07 color dot - red 150 ohms ±2%, 1/4 w, F-07 color dot - green 180 ohms ±2%, 1/4 w, F-07 color dot - gray	 932 114 022 932 114 027 932 114 029 932 114 031
R13-R20	RESISTOR, FIXED, COMPOSITION: 100 ohm ±2%, 1/4 w	932 114 036





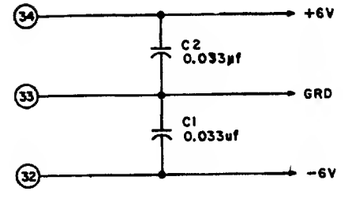


Figure A-70A. Sense Amplifier, Model CM-032, Schematic Diagram and Logic Symbol

SENSE AMPLIFIER PAC, MODEL CM-033

The Sense Amplifier PAC, Model CM-033 (Figure A-71), contains two independent sense amplifier channels which amplify the core outputs on memory sense lines and convert the information content to μ-PAC logic levels. Inputs to each channel are differential signals on twisted pair lines. The information signals (measured differentially across pins 1 and 3 for one channel and 9 and 11 for the other) are approximately 50 mv in amplitude.

A strobe input is provided which, when grounded, disables the sense amplifier channels. Strobe enable inputs are provided to gate the strobe input of the channels. An amplifier will be enabled when both the strobe and strobe enable inputs are asserted at that amplifier.

Both sense amplifier channels are provided with a direct output and a series 62-ohm termination output. The sense amplifier input ground return is generally connected to logic ground.

SPECIFICATIONS

Current Requirements

+6v: 60 ma
-6v: 40 ma
} Strobe input at ground

Threshold

Min. one signal: 45 mV
Max. zero signal: 25 mV

Circuit Delay

Strobe input (Pin 4) to output (Pins 17 and 19): 30 ± 15 ns

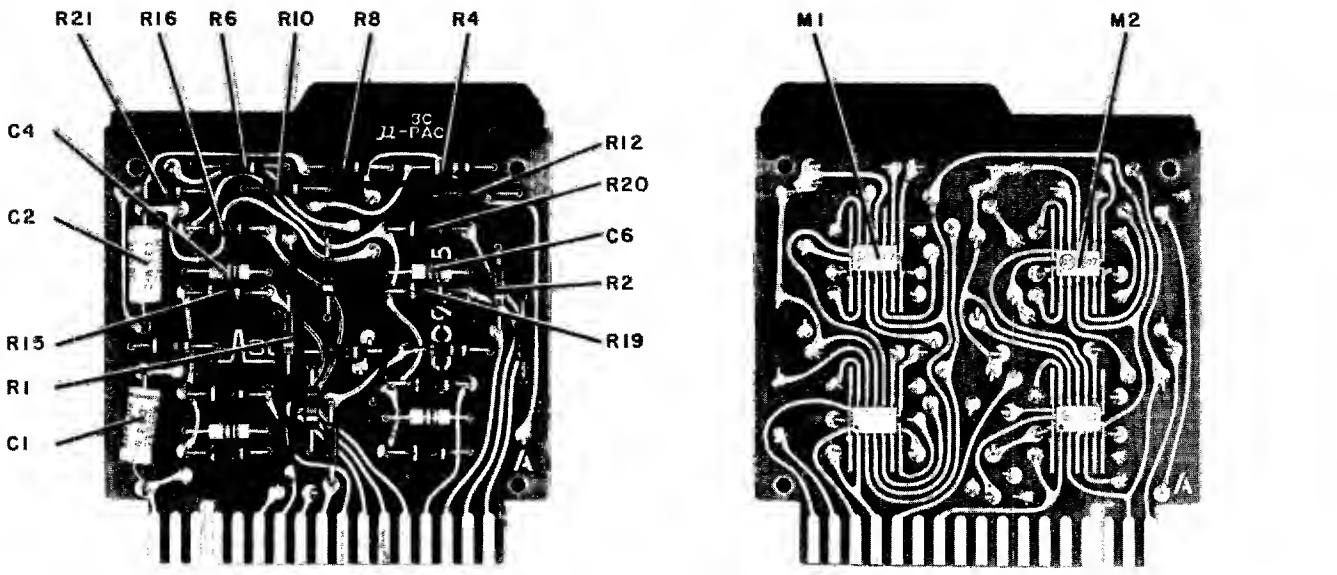


Figure A-71. Sense Amplifier PAC, Model CM-033, Parts Location

Electrical Parts List (A014391J)

Ref. Desig.	Description	Part No.
M1, M3	Deleted	
M2, M4	MICROCIRCUIT: F-07, Sense Amplifier Integrated Circuit	950 100 007
C1, C2	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±25%, 50 vdc	930 313 016
C3, C5	Deleted	
C4, C6	CAPACITOR, FIXED, CERAMIC DIELECTRIC: 47 lf ±5%, 100 vdc	930 173 111
R1, R2	RESISTOR, FIXED, COMPOSITION: 62 ohms ±5%, 1/4 w	932 007 020
R3, R5, R7, R9, R11, R13, R14, R17, R18	Deleted	
R4, R21	RESISTOR, FIXED, COMPOSITION: 3K ±2%, 1/4 w	932 114 060
R6, R8	RESISTOR, FIXED, COMPOSITION: 2K ±2%, 1/4 w	932 114 056
R10, R12	RESISTOR, FIXED, COMPOSITION: 75 ohms ±2%, 1/4 w, F-07 color dot - violet 120 ohms ±2%, 1/4 w, F-07 color dot - red 150 ohms ±2%, 1/4 w, F-07 color dot - green 180 ohms ±2%, 1/4 w, F-07 color dot - gray	 932 114 022 932 114 027 932 114 029 932 114 031
R15, R16, R19, R20	RESISTOR, FIXED, COMPOSITION: 100 ohms ±2%, 1/4 w	932 114 036

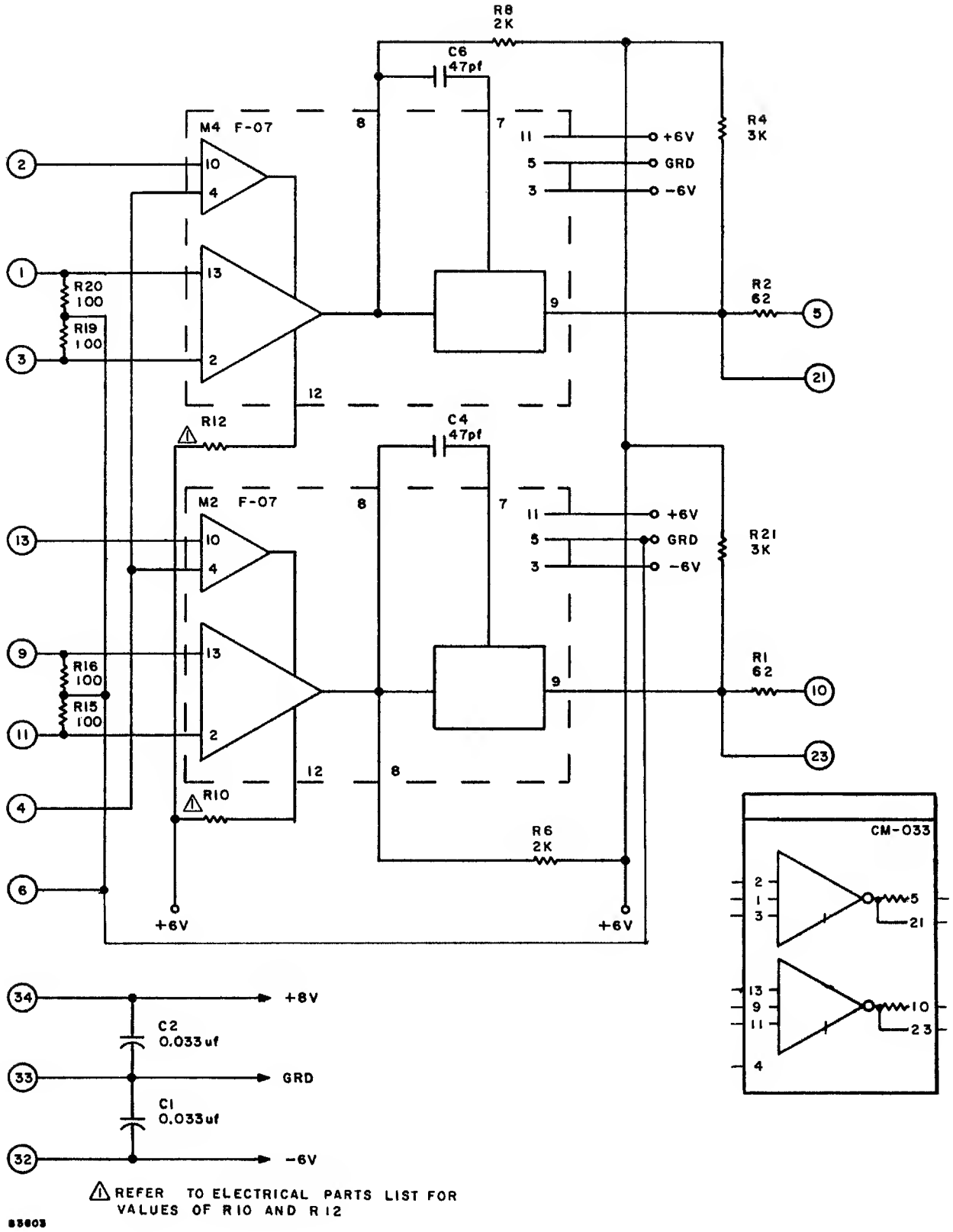


Figure A-71A. Sense Amplifier PAC, Model CM-033, Schematic Diagram and Logic Symbol

COMPONENT PAC, MODEL CM-075

The Component PAC, Model CM-075 (Figure A-72), contains 16 resistors used in microcircuit magnetic core memories for stack drive line discharge. The resistors are assembled on a DC-335 printed circuit board. One end of each resistor is wired to a stack read X-drive line. The other ends of the resistors are bussed together on the memory backplane and wired to 24v- (nominally -12 volts).

SPECIFICATIONS

Current Requirements

24v- supply: 2 ma per resistor (32 ma maximum)

Power Dissipation

640 mw maximum

Electrical Parts List

Ref. Desig.	Description	3C Part No.
R1-R16	RESISTOR, FIXED, COMPOSITION: 10 K ±5%, 1/4w	937 007 073

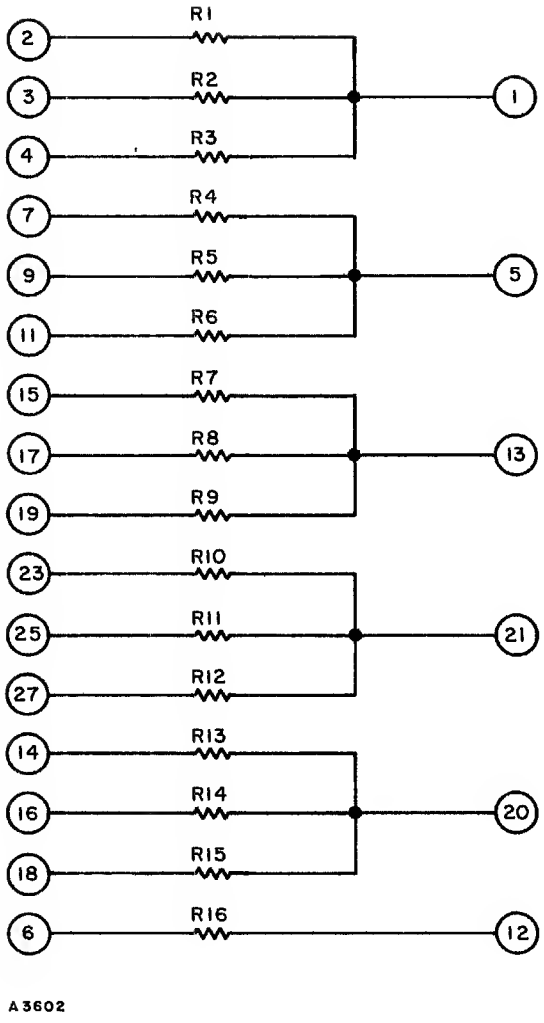


Figure A-72. Component PAC, Model CM-075, Schematic Diagram

The Other Computer Company:

Honeywell

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